Name:

Enrolment No:

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, May 2019

Course: Digital Electronics	**Semester: II**
Program: BCA	**Time: 03 hrs.**
Course Code: ECEG 2016	**Max. Marks: 100**

Instructions: Attempt all the questions

SECTION A

S. No.		Marks	CO
Q 1	Differentiate the following (a) Level-triggered and Edge-triggered flip-flops (b) Asynchronous and Synchronous counter	**4**	**CO3**
Q 2	Find the Minterms and Maxterms for the following logical expression: $F = A + B\overline{C} + AB\overline{D} + ABCD$	**4**	**CO2**
Q 3	State and Prove DeMorgan's theorem. Simplify the following expression using boolean laws: $F = \acute{A}(A+B) + (B+AA)(A+\acute{B})$	**4**	**CO2**
Q 4	Convert the following: (a) $(2598.675)_{10}$ to hexadecimal (b) $(10010.1011)_2$ to decimal (c) $(10111101.01101001)_2$ to octal (d) $(465.0647)_8$ to Binary	**4**	**CO1**
Q 5	Explain the operation of master-slave flip-flop and show how the race around condition is eliminated in it.	**4**	**CO3**

SECTION B

S. No.		Marks	CO
Q 6	What do you understand by Universal gates? Design and Implement Ex-OR and Ex-NOR gates using NAND gate.	**8**	**CO2**
Q 7	Design and implement J-K flip-flop using S-R flip-flop.	**8**	**CO3**
Q 8	Simplify the expression F(A, B, C, D) = $\Sigma\, m$ (0, 1, 5, 6, 8, 9, 13, 14) +d (3, 7, 15) using K-map and implement the result using logic gates.	**8**	**CO2**
Q 9	Differentiate weighted & non-weighted codes with suitable examples. Define even and odd parity code. Convert the following to Gray code and back to their equivalent binary code. (a) 10001110101 (b) 00101101110	**8**	**CO1**

Q10	Design a MOD-3 counter using J-K flip-flop.	**8**	**CO3**
	SECTION-C		
Q 11	(a) Design a combinational circuit that accepts a 4-bit binary number and generates a output binary number equal to the 2's complement of input number. (b) Implement the following function using 8×1 Multiplexer $F(A, B, C, D) = \Sigma (1, 3, 4, 11, 12, 13, 14, 15)$	**[10+10]**	**CO2**
Q 12	(a) Design a 4-bit synchronous down counter that counts through all states from 1111 down to 0000. (b) Design a 4-bit Self-correcting Shift Counter using D flip-flop.	**[10+10]**	**CO3**

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SECTION A

S. No.		Marks	CO
Q 1	Design and implement Full subtractor using two half subtractor.	**4**	**CO2**
Q 2	Explain with suitable truth table and logical diagram how the forbidden condition has been eliminated in J-K Flip-Flop as compared to S-R Flip-Flop.	**4**	**CO3**
Q 3	Find the value of X in the following	**4**	**CO1**

	(a) $(F3A7C2)_{16} = (X)_{10}$ (b) $(2AC5)_{16} = (X)_8$ (c) $(0.93)_{10} = (X)_8$ (d) $(4057.06)_8 = (X)_{10}$		
Q 4	State and Prove Duality principle. Simplify the following expression using boolean laws: $F = (A+C)(AD + A\acute{D}) + AC + C$	**4**	**CO2**
Q 5	Differentiate the following (a) Latch and Flip-Flop (b) Combinational and Sequential circuits	**4**	**CO3**
SECTION B			
Q 6	What do you understand by registers? Discuss with suitable logic diagram all the four configuration SISO, SIPO, PISO, PIPO of registers.	**8**	**CO3**
Q 7	Simplify the expression F(A, B, C, D) = ΠM (1, 3, 5, 8, 9, 11, 14) +d (2, 7, 10) using K-map and implement the result using logic gates.	**8**	**CO2**
Q 8	What are different types of error detecting and correcting codes. Explain with help of suitable example how the error can be detected and corrected.	**8**	**CO1**
Q 9	Design and implement D flip-flop using J-K flip-flop.	**8**	**CO3**
Q 10	What do you understand by Universal gates? Design and Implement Ex-OR and Ex-NOR gates using NOR gates.	**8**	**CO2**
SECTION-C			
Q 11	(a) Design a 4-bit Binary code to Gray code converter. (b) Differentiate multiplexer and demultiplexer. Implement the following boolean expression using a 8 X 1 multiplexer. F(A, B, C, D) = $\sum(0,1,2,5,6,9,14)$	**[10+10]**	**CO2**
Q 12	(a) Design a synchronous BCD counter using J-K flip-flops. (b) Design a 4-bit unit distance Up-Down counter using D flip-flops.	**[10+10]**	**CO3**