Name: **Enrolment No:**	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, May 2019

Programme Name: B.Tech Electronics Engineering **Semester : VIII**
Course Name : VHDL **Time : 03 hrs**
Course Code : ELEG 434 **Max. Marks : 100**
Nos. of page(s) : 02
Instructions: Assume any data in programming, if required

SECTION A (5 x 4 = 20 Marks)

S. No.	Attempt ***all*** the questions	Marks	CO
Q 1	What is entity and architecture is VHDL programming. Explain with examples.	**5**	**CO1**
Q.2	What is the concept of package in VHDL programming. Explain with example.	**5**	**CO2**
Q.3	Write the VHDL code for the positive edge triggered asynchronous T flip flop. Detail the functionality of the chip.	**5**	**CO4**
Q.4	Compare CPLD, FPGA and ASIC based on their structure.	**5**	**CO5**

SECTION B (4 x 10 = 40 Marks)

	Attempt ***all*** the questions		
Q.5	What modeling styles are followed in VHDL based design. Design the chip of 2 x 4 decoder in all style of modeling. Draw the logic diagram for the same.	**10**	**CO2**
Q.6	Design the 4-bit priority encoder or checker using VHDL. Detail the functionality of the chip with truth table and logic diagram.	**10**	**CO3**
Q.7	How behavioral model is different from data flow model. Design a (16 x 1) multiplexer chip using behavioral modeling.	**10**	**CO2**
Q.8	Detail the synthesis process on FPGA. Explain the FPGA design flow with example.	**10**	**CO5**

SECTION-C (2 x 20 = 40 Marks)

Attempt any ***two*** of the followings

Q.8 The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …. An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison. For example, a magnitude comparator of two 1-bits, (A and B) inputs would produce the following three output conditions when compared to each other. This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the case of 64-bit comparator for the different logic functions.

20 **CO3**

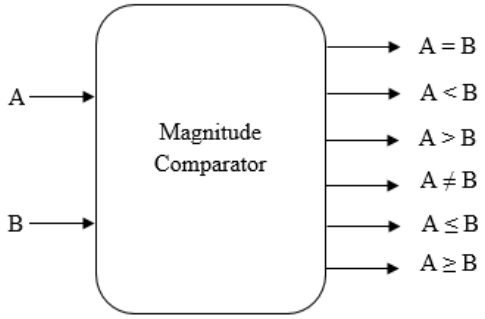
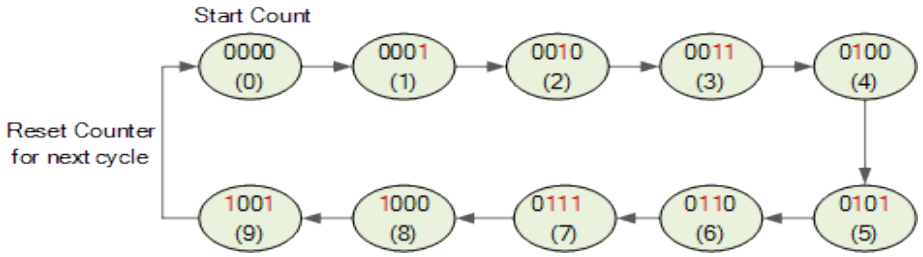
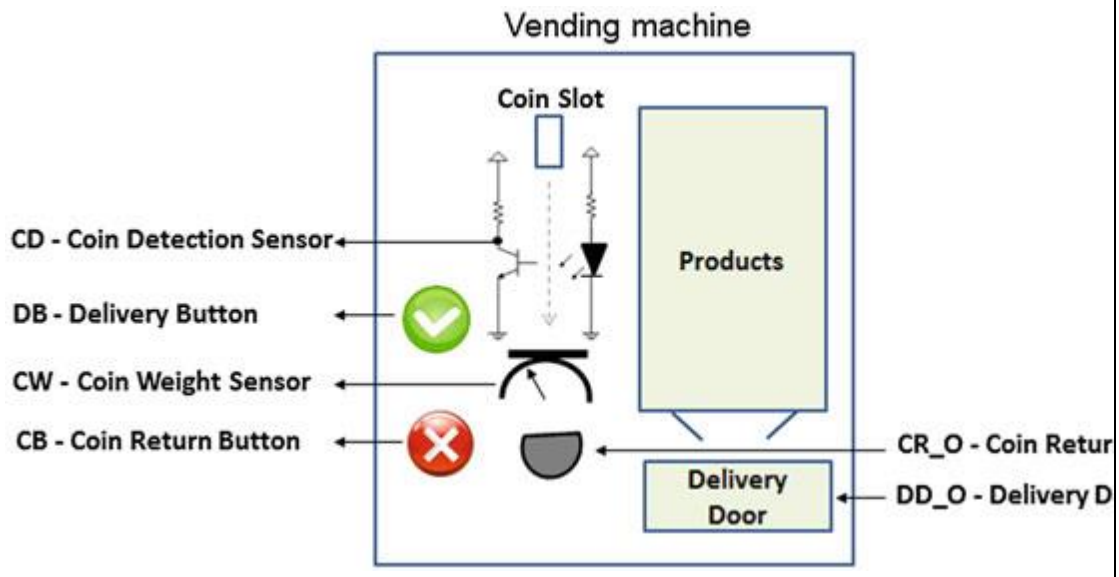


Fig.1

	(a) Develop the VHDL/ Verilog HDL code to support the functionality of design **(b)** Estimate the different test cases and test benches of the design. **(c)** Design an ALU chip that accepts 32-bit data and perform atleast 10 operations using VHDL.		
Q.9	**(a)** What is the use of enumerated data concept in VHDL. Design a 16-bit shifter using enumerated data concept that performs shift left, shift right, rotate left and rotate right operations by 1 bit. **(b)** Develop the VHDL code for the BCD counter shown below for up/down operation sequentially.  Fig, 2 BCD Counter	**10** **10**	**CO4**
Q.10	**(a)** What is the difference between Mealy and Moore FSM. Explain with example. **(b)** The vending machine has the following features (textual description): The vending machine sells just one type of product, and each product costs $0.25, Only $0.25 coins are accepted, A valid $0.25 coin weights 5.670 g, Invalid coins are rejected automatically, and the control circuit does not need to do anything about that, There is a slot to insert $0.25 coins in the vending machine, There is a coin detection circuit that outputs '1' every time a $0.25 coin is inserted in the slot, or '0' otherwise. There is a digital scale that outputs '1' when a weight of 5.670 g (or more) is detected, There is a ''delivery button'' that outputs '1' every time it is pushed. There is a ''coin return button'' that outputs '1' every time it is pushed. There is a ''coin return cup'' to collect coins ejected by the ''coin return button'' (and also rejected coins). There is a door where the user can collect their product, after have pushed the ''delivery button''. When the vending machine runs out of products, it shuts itself, and the control circuit does not need to do anything about that. Design the FSM of machine and HDL code to support the operation of machine.  Fig.3 Vending Machine	**20**	**CO5**

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SECTION B (4 x 10 = 40 Marks)

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Q.6	Design the 4-bit priority encoder or checker using VHDL. Detail the functionality of the chip with truth table and logic diagram.	**10**	**CO3**
Q.7	How structural model is different from data flow model. Design a (8 x 1) multiplexer chip using behavioral modeling.	**10**	**CO2**
Q.8	Realize a full adder using half adders and write VHDL code in structural level modeling	**10**	**CO4**

SECTION-C (2 x 20 = 40 Marks)

Attempt any ***two*** of the followings

Q.8 The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …. An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison. For example, a magnitude comparator of two 1-bits, (A and B) inputs would produce the following three output conditions when compared to each other. This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the case of 64-bit comparator for the different logic functions.

20 **CO3**

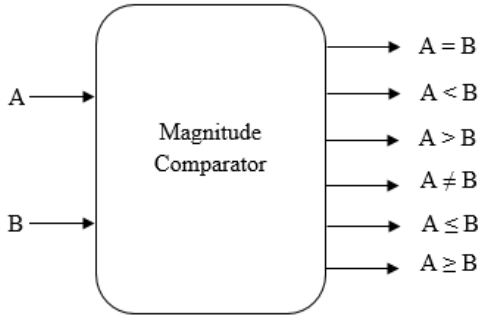
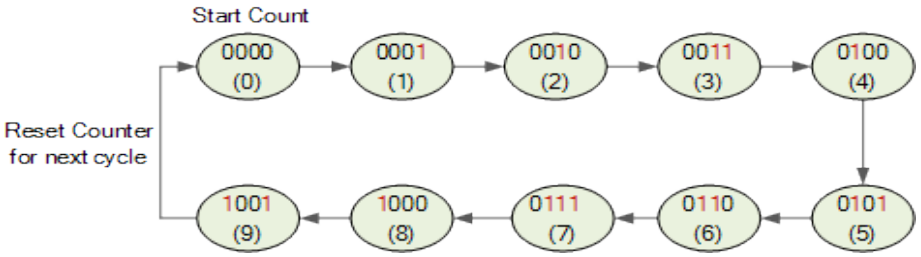
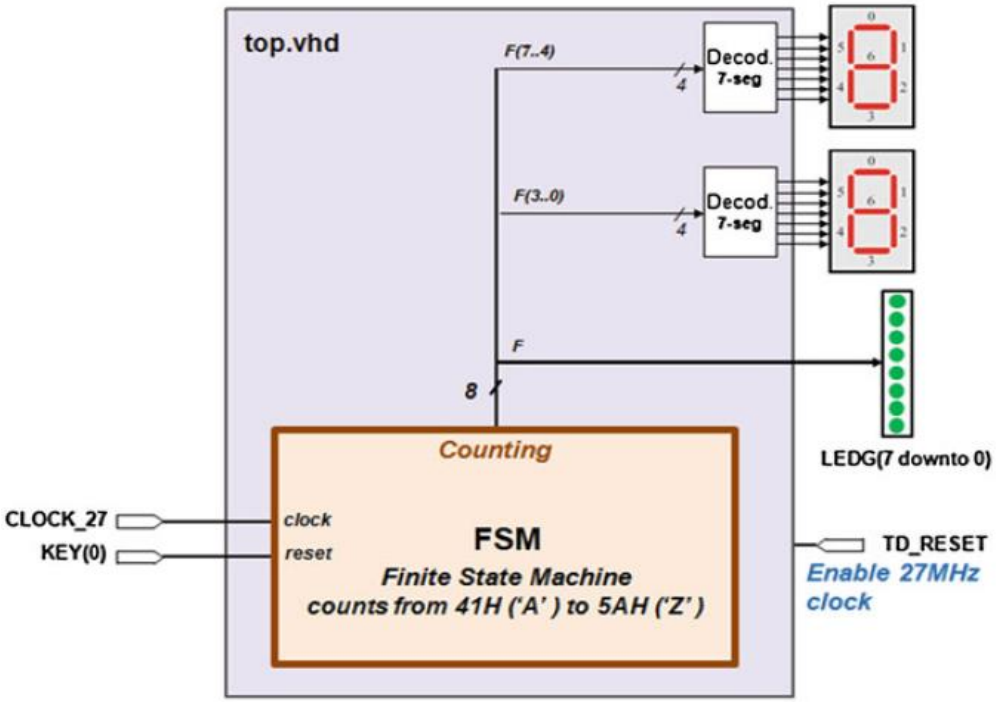


Fig.1

	(d) Develop the VHDL/ Verilog HDL code to support the functionality of design **(e)** Estimate the different test cases and test benches of the design. **(f)** Design an ALU chip that accepts 32-bit data and perform atleast 10 operations using VHDL.		
Q.9	**(a)** What is the use of enumerated data concept in VHDL. Design a 16-bit shifter using enumerated data concept that performs shift left, shift right, rotate left and rotate right operations by 1 bit. **(b)** Develop the VHDL code for the BCD counter shown below for up/down operation sequentially.  Fig, 2 BCD Counter	**10** **10**	**CO4**
Q.10	**(a) Co**mpare synchronous and asynchronous circuit. Detail the examples to support your answer. **(b)** Design and develop the VHDL code of FSM, for the generation of the ASCII characters 'A' to 'Z'. The characters should be presented on the green LEDs (binary format) and on two 7-segments displays (hexadecimal format), as shown in Fig 1The FSM should have a small number of states, but sufficient to increment the counter and check whether the final counting ('Z' = 5AH) has been reached. When the final counting is reached, the FSM should be reset to the initial state (beginning of the counting).In order to activate the DE2 27 MHz clock signal, the TD_RESET output has to be set to '1'.  Fig. 3 ASCII character display	**20**	**CO5**