Name: **Enrolment No:**	UPES UNIVERSITY WITH A PURPOSE

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2019

Course: **D**igital System Design **Semester: III**
Program: **B.Tech ECE** **Time: 03 hrs.**
Course Code: **ECEG 2028** **Max. Marks: 100**

Instructions: All diagrams to be drawn by Pencil

S. No.	QUESTION	Marks	CO
	SECTION A	**5x4=20**	
1.	Realize through NAND gates after simplification in K-Map for the function $f_1(x, y, z) = \sum(0, 1,2\ 5, 6)$	**4**	**CO1**
2.	What are the advantages of PLDs over fixed function ICs?(OR) Explain about registers in Digital logic design.	**4**	**CO2**
3.	Distinguish between latch and Flip Flop.	**4**	**CO3**
4.	What are the various methods used for triggering flip-flops? Explain with examples.	**4**	**CO4**
5.	Write about Emitter coupled logic Gate with a neat diagram.	**4**	**CO5**
	SECTION B	**4X10 =40**	
6.	Realize a Boolean function $F(w,x,y,z) = \sum(12,3, 6, 7, 12,15)$ using Multiplexer.	**10**	**CO2**
7.	Convert J-K flip-Flop into D-Flip Flop	**10**	**CO3**
8.	Design a shift register in which all the inputs are fed in parallel and outputs are collected in serial.	**10**	**CO4**
9.	Realize functions $F_1=(AB+AC+AB'C)$,$F_2=$ $(AB+B'C)'$ and $F_3 = AB' +C$ using PLA. (OR) Explain about the four types of Shift Registers.	**10**	**CO5**
	SECTION B	**2X20 =40**	
10.	(a)Design a sequential circuit for the below state diagram fig 1 using T- flip flops (b)Implement Full Adder operation using Multiplexer.	**15** **5**	**CO4**

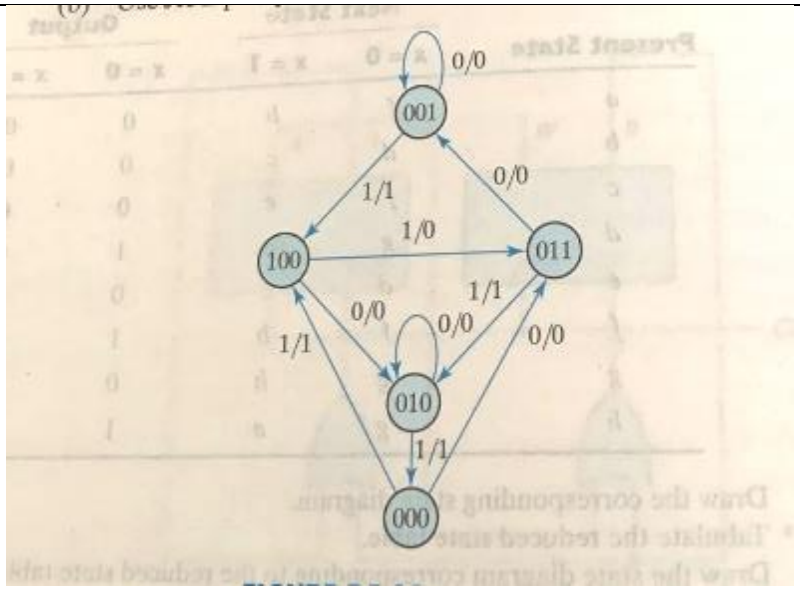

fig 1

11.	(a)Design a 4 bit universal shift register and draw the circuit with the given mode of operation table. S_1 | S_0 | Operation 0 | 0 | Shift right 0 | 1 | Shift left 1 | 0 | Parallel 1 | 1 | Inhibit clock	**10**	**CO5 & CO4**
	(b) Design a combinational circuit which give the display of the digits 0-9 and the LEDs should glow according to the binary input fed to the circuit inputs.	**10**	
	(OR) (c) Design a 16x1 Multiplexer using 4x1 Multiplexers only and illustrate the methodology to convert 16x1 Mux to four 4x1 Mux.	**8**	
	(d)Design a decimal BCD Counter using JK Flip Flops.	**12**	