Name: **Enrolment No:**	UPES UNIVERSITY WITH A PURPOSE

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2019

Course: VLSI Design **Semester: VII**
Program: **B.Tech ECE** **Time: 03 hrs.**
Course Code: **ELEG 407** **Max. Marks: 100**

Instructions: All diagrams to be drawn by Pencil

S. No.	QUESTION	Marks	CO
	SECTION A	**5x4=20**	
1.	Explain the figure of merit of a MOS transistor	**4**	**CO1**
2.	Define Fan-in and Fan-out.	**4**	**CO2**
3.	Draw the basic circuit of NMOS inverter and CMOS inverter.	**4**	**CO3**
4.	List out the limitations of scaling.	**4**	**CO4**
5.	Describe how HDL can be modelled in three different ways.	**4**	**CO5**
	SECTION B	**4X10 =40**	
6.	Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode.	**10**	**CO2**
7.	Explain how the BiCMOS inverter performance can be improved.	**10**	**CO3**
8.	Draw a layout of an expression f=(a+bc)'.	**10**	**CO4**
9.	(a)Write about test bench in VHDL programming and Distinguish test and testability. (OR) (b)What is pseudo NMOS ? Draw a NAND circuit using pseudo NMOS	**10**	**CO5** **CO4**
	SECTION B	**2X20 =40**	
10.	(a) Draw the stick diagram and mask layout for CMOS two input NAND gate. (b) Write about the lambda design rules for NMOS,PMOS , CMOS and Contact Cuts.	**10** **10**	**CO4**
11.	(a)Write a HDL for an Multiplexer for the configuration 8x1 in data flow and behavioural model	**10**	**CO5 & CO4**

	(b) Consider an NMOS in a 0.6μm process with W/L is 4/2λ(i.e. 1.2/0.6 6μm process). In this process the gate oxide thickness is 100A. and the mobility of electrons is 350 $cm^2/V \cdot S$. The threshold voltage is 0.7 V. plot I_{ds} Vs V_{ds} for the gate voltages Vgs={1,2,3,4,5}. (OR) (c)Calculate on resistance of an inverter from V_{DD} to GND. If n- channel sheet resistance Rsn=$10^4\Omega$ per square and P-channel sheet resistance Rsp = $3.5 \times 10^4\ \Omega$ per square.(Z_{pu}=4:4 and Z_{pd}=2:2). . (d)Write a HDL for an Decoder 3x8 in data flow and structural model	**10**	