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| **Name:**<br>**Enrolment No:** | UPES |

**UNIVERSITY OF PETROLEUM AND ENERGY STUDIES**

**End Semester Examination, May 2020**

**Course: Computer System Architecture** — **Semester: II**

**Course Code: CSEG2004** — **Time: 12PM-2PM**

**Programme: BCA BFSI, IOT** — **Max. Marks: 80**

**Instructions: All questions are compulsory**

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| The difference between the output states of J-K flip flop and S-R flip flop is | The S-R flip flop has invalid state | Correct | The J-K flip flop has invalid state | Incorrect | The S-R flip flop has race around condition | Incorrect | The J-K flip flop has race around condition | Incorrect |
| To implement full adder using 8:1 MUX, the no. of 8:1 MUX required are | 1 | Incorrect | 3 | Incorrect | 4 | Incorrect | 2 | Correct |
| Simplify F=x'yz + x'yz' + xz | x'y+xz | Correct | x'y'+xz | Incorrect | xy'+x'z | Incorrect | xy+x'z' | Incorrect |
| Let f(w,x,y,z)= Σ(0,4,5,7,8,9,13,15). Which of the following expressions are NOT equivalent to f? | x'y'z'+w'xy'+wy'z+xz | Correct | w'y'z'+wx'y'+xz | Incorrect | w'y'z'+wx'y'+xyz+xy'z | Incorrect | x'y'z'+wx'y'+w'y | Correct |
| Full adder circuit can be implemented by | Multiplexers | Correct | Half Adders | Incorrect | AND and OR gates | Incorrect | decoders | Incorrect |
| Register that interact with the secondary storage is _____ | MAR | Cor | PC | Incorr | IR | Incorr | R0 | Incorr |

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| | | Correct | | Correct | | Correct | |
| The minimum number of 2 to 1 multiplexers required to realize a 4 to 1 multiplexer is | 4 | Incorrect | 3 | Correct | 2 | Incorrect | 1 | Incorrect |
| The internal components of the processor are connected by _____ | Processor intra-connectivity circuitry | Incorrect | Processor bus | Correct | Memory bus | Incorrect | Ram bus | Incorrect |
| The Johnson counter is also known as | twisted ring counter | Correct | ring counter | Incorrect | Ripple counter | Incorrect | None of these | Incorrect |
| In an SR Latch made by cross coupling two NAND gates, if both S and R inputs are set to 0, then it will result in | *Q=0, Q'=1* | Incorrect | *Q=1, Q'=0* | Incorrect | *Q=1, Q'=1* | Correct | no change | Incorrect |
| ANSI stands for _____ | American National Standards Institute | Correct | American National Standard Interface | Incorrect | American Network Standard Interfacing | Incorrect | American Network Security Interrupt | Incorrect |
| The logic operations are implemented using _____ circuits. | Bridge | Incorrect | Logical | Incorrect | Combinatorial | Correct | Gate | Incorrect |
| In full adders the sum circuit is implemented using _____ | And & or gates | Incorrect | NAND gate | Incorrect | XOR | Correct | XNOR | Incorrect |
| The product of 1101 & 1011 is _____ | 10001111 | Correct | 10101010 | Incorrect | 11110000 | Incorrect | 11001100 | Incorrect |
| To increase the speed of memory access in pipelining, we make use of _____ | Special mem | Incorr | Special purp | Incorr | Cache | Cor | Buffers | Incorr |

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| | ory locations | ect | ose registers | ect | | rect | | ect |
| The result for a 4-bit parallel adder if "carry-in" is connected to HIGH is | The same as if the carry-in is tied LOW | Incorrect | That carry-out will always be HIGH | Incorrect | A one will be added to the final result | Correct | The carry-out is ignored | Incorrect |
| | significant carry-in is ignored | | | | | | | |
| What type of memory must be constantly refreshed? | DRAM | Correct | SRAM | Incorrect | VRAM | Incorrect | L1-Cache | Incorrect |
| What is the minimum number of gates required to impement the boolean function (AB+C) if we have to use only 2-input NOR gates? | 2 | Incorrect | 3 | Correct | 4 | Incorrect | 5 | Incorrect |
| How many full adders are required to construct an m-bit paraller adder? | m | Correct | m-1 | Incorrect | m/2 | Incorrect | m+1 | Incorrect |
| Acombinational circuit consists of | Logic gates and a memory element | Incorrect | Memory elements only | Correct | Logic gates only | Incorrect | None of these | Incorrect |
| The number of NOR gates required to implement EX-NOR gate | 4 | Correct | 3 | Incorrect | 5 | Incorrect | 6 | Incorrect |
| To convert a full adder into a full subtractor | one input to carry | Correct | carry is to be comp | Incorr | sum is to be compl | Incorr | cannot be converted | Incorr |

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| | is to be complemented | | lemented | ect | emented | ect | | ect |
| The fetching, decoding and executing of an instruction is broken down into several time intervals. Each of these intervals, involving one or more clock period is called a | Instruction cycle | Incorrect | Process cycle | Incorrect | Machine cycle | Correct | None of these | Incorrect |
| The operation of gate is commutative but not associative is | NOR | Correct | EX-OR | Incorrect | OR | Incorrect | AND | Incorrect |
| In a sequential circuit, the outputs at any instant of time depends | only on the inputs present at that instant of time | Incorrect | on past outputs as well as present inputs | Correct | only on the past inputs | Incorrect | only on the present outputs | Incorrect |
| How many flip flops are required to build a binary counter circuit to count from 0 to 2048? | 10 | Incorrect | 9 | Incorrect | 11 | Correct | 8 | Incorrect |
| The master slave JK flip flop is effectively a combination of | a T and D flip flop | Incorrect | SR and a D flip flop | Incorrect | SR and T flip flop | Correct | two T flip flop | Incorrect |
| An SR Latch is a | combinational circuit | Incorrect | synchronous sequential circuit | Incorrect | one bit memory element | Correct | one clock delay element | Incorrect |
| The present output $Q_n$ of an edge triggered JK flipflop is logic 0. If J=1, then | will be logic 0 | Incorrect | will be logic 1 | Correct | cannot be determined | Incorrect | will race around | Incorrect |
| The registers in which data can be shifted serially or parallelly are known as _____. | Serial in-Serial Out | Incorr | Serial in-Parallel | Incorr | Parallel in-Parallel Out | Incorr | Shift Registers | Correct |

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| | Registers | ect | Out Registers | ect | Registers | ect | | |
| Basic 4-bit shift register can be constructed using | four D flip flops | Correct | four T flip flops | Incorrect | two D flip flops | Incorrect | three D flip flops | Incorrect |
| On the third clock pulse, a 4-bit Johnson sequence is $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, and $Q_3 = 0$. On the fourth clock pulse, the sequence is _____. | $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 1$ | Correct | $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 0$ | Incorrect | $Q_0 = 1$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$ | Incorrect | $Q_0 = 0$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$ | Incorrect |
| Computers operate on data internally in a _____ format. | tristate | Incorrect | universal | Incorrect | serial | Correct | parallel | Incorrect |
| In a 4-bit Johnson counter sequence there are a total of how many states, or bit patterns? | 1 | Incorrect | 2 | Incorrect | 4 | Incorrect | 8 | Correct |
| Hexadecimal value of binary 111111110010 is | $EE2_{16}$ | Incorrect | $FF2_{16}$ | Correct | $2FE_{16}$ | Incorrect | $FD2_{16}$ | Incorrect |
| In digital electronics voltages are continously variable | FALSE | Correct | TRUE | Incorrect | | | | |
| Most computers store data in strings of _____ bits called a _____ | 8, word | Incorrect | 16, word | Incorrect | 16 byte | Incorrect | 8 byte | Correct |
| In which addressing mode the operand is giving explicitly in the instruction | Absolute | Incorrect | Direct | Incorrect | Indirect | Incorrect | Immediate | Correct |
| _____ addressing mode is most suitable to change the normal sequence of execution of instructions. | Relative | Correct | Indirect | Correct | Index with offset | Incorrect | Immediate | Incorrect |

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| _____ stores the decoded instruction. | IR | Correct | PC | Incorrect | Registers | Incorrect | MDR | Incorrect |
| Data in SRAM does need not to be refreshed dynamically. | TRUE | Correct | FALSE | Incorrect | | | | |
| Characteristics of Auxilliary memory are | Reliable | Incorrect | Reusable | Incorrect | Cost | Incorrect | All of the above | Correct |
| Which of the following are not magnetic storage? | Floppy disk | Incorrect | CD-ROM | Correct | Magnetic tape | Incorrect | Hard disk | Incorrect |
| Interrupts are initiated by _____ instruction. | Internal | Incorrect | External | Correct | Hardware | Incorrect | Software | Incorrect |
| When interrupt signaled, processor executes a routine called as _____ | Interrupt handler | Correct | Interrupt cycle | Incorrect | Interrupt device | Incorrect | None of these | Incorrect |
| It is the part of operating system and determines the action to be taken. | I/O handler | Incorrect | INT handler | Correct | Both of these | Incorrect | None of these | Incorrect |
| _____ are used as operands. | Input | Incorrect | Data | Correct | Information | Incorrect | Stored Values | Incorrect |
| Polling leads to the CPU wastage. | TRUE | Correct | FALSE | Incorrect | | | | |
| CAR stands for | Control Address Register | Correct | Central Address Register | Incorrect | Circuit Adress Register | Incorrect | None of these | Incorrect |

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| SDRAM stands for | Synchronous Dynamic Access Memory | Correct | Sequential Dynamic Aces Memory | Incorrect | Serial Dynamic Access Memory | Incorrect | None of these | Incorrect |
| How can the processor ignore other interrupts when it is servicing one | By turning off the interrupt request line | Incorrect | By disabling the devices from sending the interrupts | Incorrect | By using edge-triggered request lines | Incorrect | All of the above | Correct |
| The interrupt servicing mechanism in which the reqesting device identifies itself to the processor to be serviced is | Polling | Incorrect | Vectored interrupts | Correct | Interrupt nesting | Incorrect | Simultaneous requesting | Incorrect |
| Arrange the following from fastest to lowest speed : A) Main Memory B) Cache Memory C) CPU registers D) Auxilliary Memory | D-C-A-B | Incorrect | C-A-D-B | Incorrect | D-A-B-C | Correct | B-C-D-A | Incorrect |
| Which of the following are types of Associative Memory? | Hetero Associative | Incorrect | Auto associative | Incorrect | None of these | Incorrect | Both of these | Correct |
| CISC is an acronymn for | Common Instruction Set Computer | Incorrect | Complex Instruction Set Computer | Correct | Circuit Instruction Set Computer | Incorrect | None of these | Incorrect |
| Convert (14.34) base 10 into binary | 1011.1101 | Incorrect | 1110.1001 | Incorrect | 1110.0101 | Incorrect | 1011.01001 | Correct |

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| Let A=1111 1010 and B=0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is: | 11000100 | Correct | 10011100 | Incorrect | 10100101 | Incorrect | 11010101 | Incorrect |
| The 2's complement representation of -17 is | 101110 | Incorrect | 111110 | Incorrect | 101111 | Correct | 110001 | Incorrect |
| A Boolean function x'y' + xy + x'y is equivalent to: | x' + y' | Incorrect | x + y | Incorrect | x + y' | Incorrect | x' + y | Correct |
| The switching expression corresponding to f(A,B,C,D) = Σ(1,4,5,9,11,12) | BC'D'+A'C'D+AB'D | Correct | ABC'+ACD+B'C'D | Incorrect | ACD'+A'BC'+A'C'D' | Incorrect | A'BD+ACD'+BCD' | Incorrect |
| Flip flops will be used for clock circuits and latches are used for asynchronous. | TRUE | Correct | FALSE | Incorrect | | | | |
| Transparent latches can also be called as | Full flip flops | Incorrect | Half flip flops | Correct | Level flip flops | Incorrect | Half latches | Incorrect |
| Which of the following is the characteristic of RAM? | Slow | Incorrect | Unreliable | Incorrect | Volatile | Correct | Bulky | Incorrect |
| _____ is used to store one bit of data. | Registers | Incorrect | Flipflops | Correct | Encoder | Incorrect | Decoder | Incorrect |
| Von Neumann architecture is | SISD | Correct | SIMD | Incorrect | MIMD | Incorrect | MISD | Incorrect |
| MIMD Stands for | Multiple Instruction Multi | Correct | Multiple Instruction Mem | Incorrect | Memory Instruction Multi | Incorrect | Memory Instruction Mem | Incorrect |

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| | ple Data | | ory Data | | ple Data | | ory Data | |
| Combinational Logic circuit that sends data coming from single source to two or more destinations is | Decoder | Incorrect | Encoder | Incorrect | Multiplexer | Incorrect | Demultiplexer | Correct |
| A source program is usually in _____ | Assembly language | Incorrect | Machine level language | Incorrect | High-level language | Correct | Natural language | Incorrect |
| PC is also called as | Instruction pointer | Correct | Memory Pointer | Incorrect | Data counter | Incorrect | File pointer | Incorrect |
| The register that keeps track of the instructions in the program stored in memory is: | Control Register | Incorrect | Program Counter | Correct | Status Register | Incorrect | Direct Register | Incorrect |
| During the execution of a program which gets initialized first ? | IR | Incorrect | PC | Correct | MAR | Incorrect | None of these | Incorrect |
| NOT gate operation can also be called as | inverting | Correct | converting | Incorrect | reversing | Incorrect | reverting | Incorrect |
| In basic computer ____ bit of the instruction specifies the_____. | 15, addressing mode | Correct | 16, opcode | Incorrect | 15, opcode | Incorrect | 16, addressing mode | Incorrect |
| Scratch register to store intermediate results is known as | Permanent Register | Incorrect | Regular Register | Incorrect | Temporary Register | Correct | None of these | Incorrect |
| MIPS stands for | Multiple Instructions executed per second | Incorrect | Million Instructions executed Per | Correct | Memory Instructions executed Per second | Incorrect | None of these | Incorrect |

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| If more than one adder is available in a CPU, all adders can work simultaneously for consecutive instructions. The technique is known as | Multi Scalar Architecture | Incorrect | Second SuperScalar Architecture | Correct | Both of these | Incorrect | None of these | Incorrect |
| The Input Register (INPR) holds an _____ bit character gotten from an input device. | 4 | Incorrect | 6 | Incorrect | 8 | Correct | 10 | Incorrect |
| _____ is a Universal gate. | NOR gate | Incorrect | NAND gate | Correct | NOT gate | Incorrect | AND gate | Incorrect |
| To store data in a computer the 8 bit encoding format used is _____ | ASCII | Incorrect | EBCDIC | Correct | ANCI | Incorrect | USCII | Incorrect |
| A logical function of three variables is given as f(A,B,C)=(A+BC)(B+C'A). The canonical SOP form is: | ∑(2,4,8,10) | Incorrect | ∑(2,4,6,7) | Incorrect | ∑(3,5,8,9) | Incorrect | ∑(3,4,6,7) | Correct |