Name: **Enrolment No:**	UPES UNIVERSITY WITH A PURPOSE

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
Online End Semester Examination, Dec 2020

Course: Computer System Architecture **Semester: V**
Program: B. Tech. CSE + L.L.B (hons.) Cyber Law **Time 03 hrs.**
Course Code: CSEG 2004 **Max. Marks: 100**

SECTION A

1. **Each Question will carry 5 Marks**
2. **Numerical answer type you have to writhe the correct answer in the text box and Multiple choice question answer type in the correct option in the text box.**

S. No.	**Question**	**CO**	
Q 1	Minimized expression of the following Boolean function- F (A, B, C, D) = Σm (0, 1, 2, 5, 7, 8, 9, 10, 13, 15) a).BD + C'D + B'D' b).BB+CD+BD c). AB+BC+CA d). B'D + C'D' + B'D'	**CO1**	**5**
Q2	(Numerical answer type) Provide the reverse polish notation for the following expression ($ is symbol to represent the end of the stack) ((3^2 - 4*1*2)^(1/2) - 3)/(2*1)$	**CO2**	**5**
Q3	Calculate the pipelining speed up in the following scenario. 4 stage pipeline system, with stage delay of 20 ns and total 1000 instructions to be executed. a).3.00 b).4.88 c).3.88 d). 4.00	**CO4**	**5**
Q4	(Numerical answer type) Consider a pipelined machine with 6 execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, and 50 ns and pipelining delay of 5ns. - What is the instruction latency on the pipelined machine? - How much time does it take to execute 100 instructions?	**CO4**	**5**

Q5	Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively a).10,17 b).10,22 c).15,17 d).5,17	**CO5**	**5**
Q6	Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line? (Considered Daisy Chaining) a). Neither vectored interrupt nor multiple interrupting devices are possible. b). Vectored interrupts are not possible but multiple interrupting devices are possible. c). Vectored interrupts and multiple interrupting devices are both possible. d) Vectored interrupt is possible but multiple interrupting devices are not possible.	**CO2**	**5**
SECTION B **1. Each question will carry 10 marks** **2. Instruction: Write short answer and use diagrams whenever necessary.**			
Q 7	Write in brief about the instruction cycle and machine cycle and also provide the details about the instruction format with example.	**CO3**	**10**
Q 8	Provide the circuit diagram and characteristics equation of JK flip flop or RS flip flop.	**CO1**	**10**
Q 9	Discuss control unit. Differentiate between microprogrammed and Hardwired control unit.	**CO2**	**10**
Q 10	Compare, strobe and handshaking of data transfer for I/O devices with diagram.	**CO5**	**10**
Q 11	Discuss the daisy chaining approach for handling interrupts in detail with the help of a proper diagram.	**CO5**	**10**
Section C **1. Each Question carries 20 Marks.** **2. Instruction: Write long answer.**			
Q12	a). Discuss the functionality of encoder decoder. b). Draw the circuit for 4:1 MUX. c). Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. Find the number of bits in the TAG, LINE and WORD fields. OR	**CO1, CO5**	**20 [6+10+4]**

	a). Discuss the functionality of MUX and DEMUX with example. b). Draw the complete circuit of 2 to 8 decoder with truth table. c). Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8.	**OR** **[4+4+6+6]**	