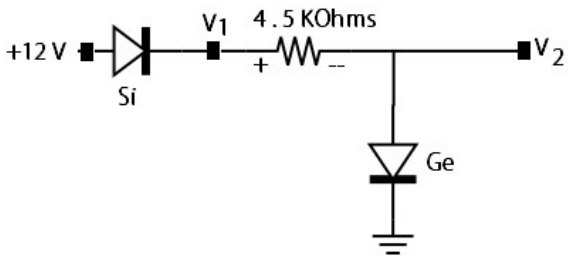
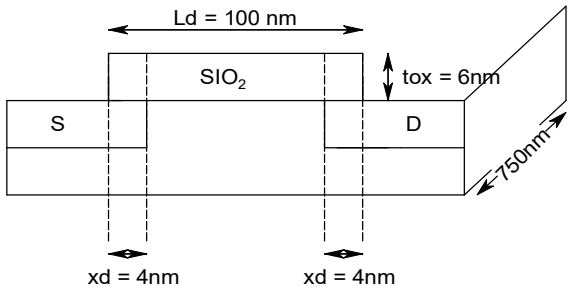
Name: Enrolment No:	UPES

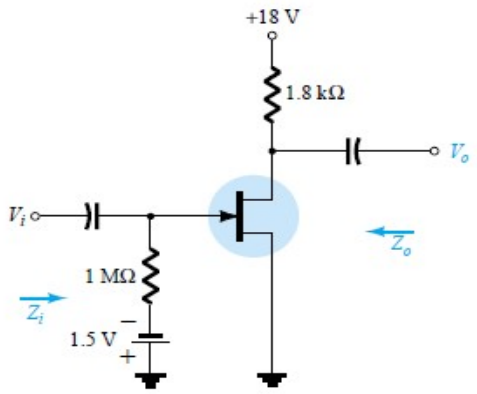
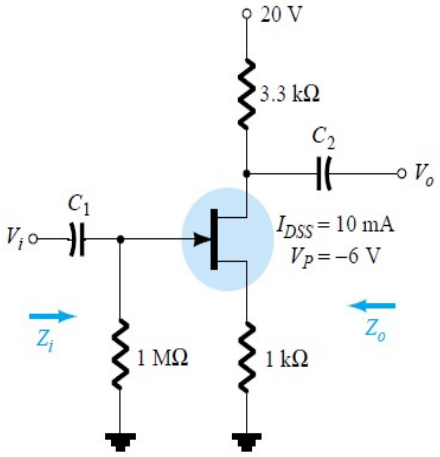
UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, Dec 2020

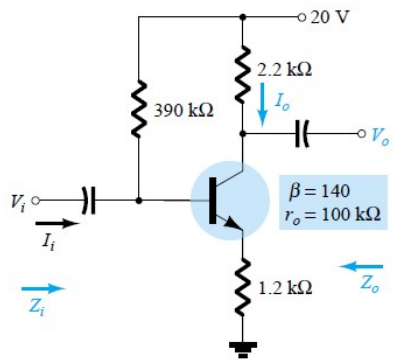
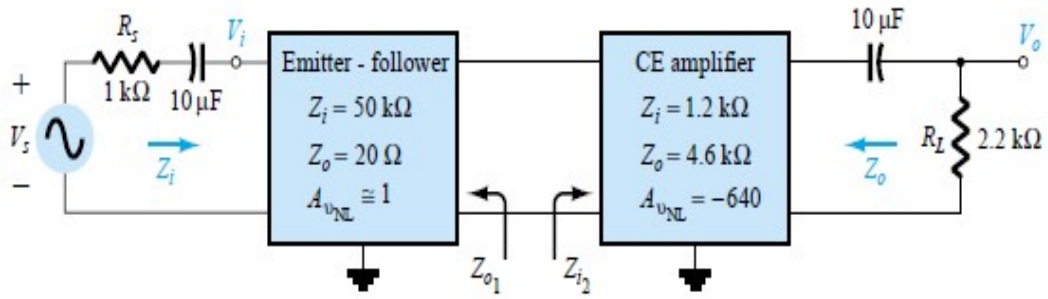
Programme Name: B.TECH ECE **Semester: III**
Course Name: Analog Electronics I **Time: 03 hrs**
Course Code: ECEG 2011 **Max. Marks: 100**
Nos. of page(s): 2
Instructions: All questions are compulsory

SECTION A

S. No.		Marks	CO
Q 1	Fill in the Blanks 1.a The input Impedance of amplifier should be very ……as possible. 1.b Emitter follower configuration has……..voltage gain. 1.c CE configuration output is differ by ……. Phase shift. 1.d For switching action of BJT the biasing region of the BJT should be in…….. region	**5**	**CO1**
Q 2	For the circuit shown in fig 1, determine $\mathbf{V_1}$ and $\mathbf{V_2}$  Fig. 1	**5**	**CO1**
Q 3	Define the thermal runaway condition in BJTs and why FET are more preferable over BJTs.	**5**	**CO2**
Q 4	Why the DC operating point is preferred to get biased at middle of DC load line.	**5**	**CO1**
Q5	**Choose the correct answer (MCQ type):** **5.**1 The action of JFET in its equivalent circuit can best be represented as a A. Current controlled Current source B. Current controlled voltage source C. Voltage controlled voltage source D. voltage controlled current source **5.2 The current gain of a bipolar transistor drops at high frequencies because of**	**5**	**CO2**

	A. Transistor capacitances B. High current effects in the base C. Parasitic inductive elements D. The early effect **5.3** Most of the linear ICs are based on the two-transistor differential amplifier because of its A. Input voltage dependent linear transfer characteristic B. High voltage gain C. High input resistance D. High CMRR		
Q6	How temperature affects the performance of the Amplifier and what is the role of different biasing configuration used for amplification network.	**5**	**CO3**
	SECTION B		
Q7	Compute the Gate capacitance CG, gate to drain capacitance CGD, gate to source capacitance for the Fig. 1. Consider the overlapping capacitances CGSO = CGDO = 5 fF/m^2 .What will be effects on these capacitances when horizontal dimension are scaled by 1/4 and vertical dimensions by 1/3.  **Fig. 1**	**10**	**CO2**
Q 8	The fixed-bias configuration shown in Fig. 2 having an operating point defined by V_{GSQ} = 2 V and I_{DQ} =5.625 mA, with I_{DSS} = 10 mA and V_{GSOFF} = -8 V. The network is redrawn as Fig with an applied signal *Vi*. The value of y_o is provided as 50 uS. (a) Determine *gm*. (b) Find *rd*. (c) Determine *Zi*. (d) Calculate *Zo*. (e) Determine the voltage gain *Av*.	**10**	**CO3**

	 Fig. 2		
Q9	A self bias configuration is shown in Fig. 3 has an operating point defined by V_{GS} = -2.6 V and I_{DQ} = 2.6 mA. Determine the followings for yos is given as 20 µS a. Tranconductance b. Rd c. Zi d. Compute Av with and without effects of rd. compare the results  **Fig. 3**	**10**	**CO3**
Q10	(a) Determine the operating point of the given amplifier as shown in Fig 4 under DC analysis? Evaluate the following performance parameters of the given CE amplifier below (b) Find *Zi* and *Zo*. (c) Calculate *Av* and *Ai*.	**10**	**CO2**

	 Fig. 4		
Q11	Differentiate between Enhancement type and Depletion type MOSFET? Why it is considered high input impedance for the amplification action and how MOSFETs are suitable for this action.	**10**	**CO4**
	SECTION-C		
Q 12	Consider the cascade amplifier configuration for Common emitter of figure given below, determine the following? : (a) The loaded voltage gain of each stage. (b) The total gain of the system, Av. (c) The total gain of the system, Ai. 	**20**	**C04**