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| **Name:**<br>**Enrolment No:** | UPES |

# UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

## End Semester Examination, December 2020

**Programme Name:** B. Tech (Electronics Engineering) **Semester** : VII
**Course Name** : VLSI Design **Time** : 3:00 hrs
**Course Code** : ECEG-4001 **Max. Marks:** 100
**Nos. of page(s)** : 02
**Instructions:** Assume any data in programming, if required.

**SECTION A (6 x 5 = 30 Marks)**

**Attempt *all* the questions**

**Q.1** Compare NMOS and PMOS based on their performance parameters. [5] [CO1]

**Q.2** Write the all steps in the FPGA Design flow. [5] [CO4]

**Q.2** Write the all steps in ASIC Design flow and synthesis. [5] [CO4]

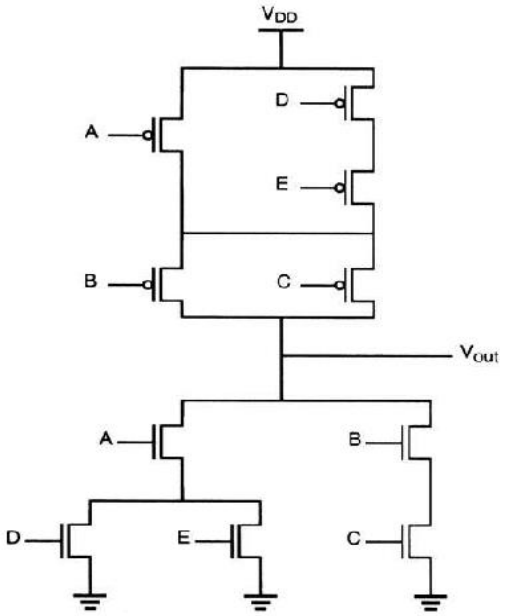
**Q.4** Detail the logic simulation of asynchronous positive edge D Flip-flop using VHDL. [5] [CO5]

**Q.5** Explain the Noise Margin and speed of operation of digital circuits. A logic gate is defined by the following volatge levels

$$V_{OH} = 5\ V$$
$$V_{OL} = 0.2\ V$$
$$V_{IH} = 2.5\ V$$
$$V_{IL} = 0.8\ V$$

Find the noise margin of this gate. [5] [CO3]

**Q.6** Write the output of the logic diagram shown below and justify your answer. [5] [CO3]



## Section-B (5 x 10 = 50 Marks)

**Attempt *all* the questions**

**Q.7** Detail the functionality of enhancement type NMOS under different regions. Derive the mathematical equations of the drain current for NMOS in all the regions. [10] [CO1]

**Q.8** Write the detailed steps in CMOS fabrication using N-well process. [10] [CO2]

**Q.9** Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA. [10] [CO4]

**OR**

Detail the followings with respect to MOSFET circuits
(a) Noise Margin in CMOS
(b) Power delay product
(c) Propagation delay
(d) Speed of operation

**Q.10** Draw the voltage transfer curve for the NMOS inverter and derive the mathematical expression to estimate the value of $V_{OH}$, and $V_{IL}$ for NMOS inverter circuit and detail the functionality. [10] [CO3]

**Q.11** Draw the CMOS logic layout and stick diagram of 2 input NOR and XOR gates. [10] [CO3]

**OR**

Design a Full adder using VHDL Programming in data flow and behavioral model.

## Section-C (1 x 20 = 20 Marks)

**Q.12** An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory. An ALU performs basic arithmetic and logic operations. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logic operations are comparisons of values such as NOT, AND, and OR. All information in a computer is stored and manipulated in the form of binary numbers, i.e. 0 and 1. Transistor switches are used to manipulate binary numbers since there are only two possible states of a switch: open or closed. An open transistor, through which there is no current, represents a 0. A closed transistor, through which there is a current, represents a 1.Operations can be accomplished by connecting multiple transistors. One transistor can be used to control a second one in effect, turning the transistor switch on or off depending on the state of the second transistor. This is referred to as a gate because the arrangement can be used to allow or stop a current.
***Develop the code for 32- bit ALU chip design that performs any 15 operations using any HDL.***

**[20] [CO5]**

**OR**

**Q.12 (a)** Design the 4 x 1 multiplexer using dataflow and behavioral model. Detail the logic synthesis and simulation using different test cases.
**(b)** Design a 3 x 8 Decoder chip using behavioral model. Detail the logic synthesis and simulation using different test cases. **[20] [CO5]**