Name: **Enrolment No:**	UPES UNIVERSITY WITH A PURPOSE

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, May 2021

Course: Computer Organization & Architecture **Semester: VI**
Program: B.Tech Mechatronics Engg. **Time: 03 hrs.**
Course Code: EPEG 2005 **Max. Marks: 100**
Instructions: All questions are compulsory

SECTION A

S. No.		Marks	CO
Q 1	Which of the following statements for intel 8085 is correct? a. Program Counter (PC) specifies the address of the instruction last executed. b. PC specifies the address of the next instruction to be executed. c. PC specifies the address of the instruction being executed. d. PC specifies the number of instructions executed so far.	**5**	**CO3**
Q 2	A processor has 43 address lines. The amount of memory that can be connected to the processor is _____. a. 64 GB b. 1024 B c. 256 B d. 8 TB	**5**	**CO3**
Q 3	Which of the following is an 8085 hardware interrupt? a. TRAP. b. RST6.5 c. RST7.5 d. ALL	**5**	**CO3**
Q 4	A direct memory address (DMA) implies_____ a. Direct transfer of data between memory and accumulator. b. Direct transfer of data between memory and I/O devices without the use of microprocessor. c. Transfer of data exclusively within microprocessor registers. d. A fast transfer of data between microprocessor and I/O devices.	**5**	**CO4**
Q 5	Explain 2D and $2\frac{1}{2}$ DRAM organization.	**5**	**CO2**
Q 6	Explain microprogram sequencing.	**5**	**CO1**

SECTION B

Q 7	Find the expression for generation of carry in four bit carry look ahead adder. Also draw its logic diagram	**10**	**CO1**
Q 8	Explain the operation of status or flag register in 8085 microprocessor.	**10**	**CO3**
Q 9	Explain the stack operations of the processor. Discuss the Reverse Polish notation concept of stack operation.	**10**	**CO2**

Q 10	What is addressing modes? Explain all addressing modes of 8085 microprocessor.	**10**	**CO3**
Q 11	Explain the concept of virtual memory and memory organization.	**10**	**CO4**
SECTION-C			
Q 12	a) Define the parallel processing. Give the Flynn's classification of parallel processors. b) Discuss various organizations of RAM. A computer uses RAM chips of 1024 *2 capacities. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?	**15+5**	**CO4**