IMPACT OF SEPIC TOPOLOGY OVER RENEWABLE POWER TRANSMISSION

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APPENDIX – III

A Declaration by the Guide

This is to certify that the **Mr Saurabh Pandey** a student of **MBA POWER MANAGEMENT** SAP ID **500071994** of UPES has successfully completed this dissertation report on **IMPACT OF SEPIC TOPOLOGY OVER RENEWABLE POWER TRANSMISSION** under my supervision.

Further, I certify that the work is based on the investigation made, data collected and analysed by him and it has not been submitted in any other University or Institution for award of any degree. In my opinion it is fully adequate, in scope and utility, as a dissertation towards partial fulfilment for the award of degree of MBA.

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LIST OF SYMBOLS, ABBREVIATION AND NOMENCLATURE

S	Power MOSFET switch
D	Flywheel diode
C	Capacitor
L	Inductor
V_{in}	Input voltage
V_o	Output voltage
I_{In}	Input current
I_{out}	Output current
R_L	Load resistance
i_L	Inductor current
v_L	Inductor voltage
D	Duty cycle
T_{on}	Switch ON time
T	Total time period
S_S	Switching stress
I_j	The rms current applied to switch j
V_j	The peak voltage applied to switch j
U	Switch utilization
I_C	Collector current
$P_{V,COND}$	Conduction power loss
T_A, T_B, T_C	Three known temperatures
$k(I_c)$	Switching-loss factor

E_{Total}	Total switching energy loss
T_J	Temperature of junction
ZVS	Zero-voltage switching
ZCS	Zero-current switching ZCS
i_{fw}	Freewheeling current
i_{L1}	Currents in L_1
i_{L2}	Currents in L_2
K_a	Conduction parameter
$K_{a(crit)}$	Critical conduction parameter
M	Output-to-peak-input ratio
n	Transformer turn ratio.
t_{don}	ON time of the output diode ($d_{don}= t_{don}/T_s$)
t_{on}	ON time of the switch ($d_{on}= t_{on}/T_s$)
t_{off}	OFF time of both switch and output diode
T_s	Switching period
v_1, i_1 (v_{1r}, i_{1r})	Input voltage and current; rectified input voltage and current
v, i_o	Ouput voltage and current

CHAPTER 1

INTRODUCTION

The beginning and pervasive accessibility of reliable and efficient standard power modules has considerably changed the focus of the power conversion. In the days of centralized custom power supplies, we needed to understand the details of converter operation, such as selection of converter topology, operating frequency and components. The need for this level of detailed knowledge about the internal workings of the converter is largely eliminated when using standard modules and we can direct our time and energy to system related issues. Most of the converter topology choices will be transparent to the end user - that is, the specifications of the module and its performance in the end system will not be affected.

There are some choices, however, that will change performance and the system designer should be familiar with these considerations. The 1999 introduction of synchronous or active rectification in power modules has significantly improved efficiency, one of the most important system considerations. Multi-phase or interleaved topologies have an effect on dynamic response, system decoupling requirements and converter form factor. We should have enough knowledge of the trade-offs associated with these types of design decisions to make an intelligent selection of power modules.

SEPIC converter is basically a DC to DC converter device which is used to step up or step down the DC voltage.

In this section we will review why power conversion is such a universal requirement in today's electronic systems. In renewable energy resources such as solar energy we use solar cell. The output of solar cell is very less, which may be the cause of power loss in transmission of power. To rectify this problem, we have introduced SEPIC converters. We will define the difference between up conversion and down conversion and

distinguish between the two circuit techniques used for power conversion - linear and switch mode regulation.

1.1 The Need for Power Conversion

Nowadays solar power generation is very easy, but the transmission and distribution of solar power is quite tough because there are many factors which can cause of loss in solar power. if the power is transmitted in very low voltage then it can cause a power loss in the transmission line. To reduce this loss of power, SEPIC converter helps a lot. Another name of SEPIC converter is BUCK BOOSTER. It boosts their voltage which can help to reduce the power losses in the transmission of DC power.

Nowadays the application of dc-dc converters plays a very important role in power electronics. In many dc applications we need to step up or step down the input voltage level. To step up or step down the voltage level we have lots of dc-dc converters. In this dissertation we analyze the performance of a modified SEPIC converter. The modified SEPIC circuit offers lower conduction losses with reduced components at the same time. The enhancement of circuit topology and performance has been achieved by integrating the two inductors into a single magnetic core. It also makes an additional reduction in SEPIC converter size.

With the exclusion of the simplest battery powered devices, all electronic equipment requires some sort of power conversion. Electronic circuitry operates from dc voltage sources while power delivery to the user's system is in the form of ac power. Furthermore, the end circuitry design is optimized to operate from specific levels of dc voltage so that more than one value of dc voltage is needed in most systems. The latest ICs now require dc voltages as low as 1V, while some circuitry operates at dc voltages up to 100V. The various dc voltage levels sometimes must be sequenced or controlled so that they can be turned on and off in a desired way. For most equipment, galvanic isolation of the dc voltages from the powerline is needed to meet international safety standards. Other standards define the interface between the powerline and the power converter(s). These types of requirements define the need for dc/dc converters. To summarize, almost all electronic equipment uses power conversion in one form or

another. The power converter performs several functions, and the virtual importance of these functions will sometimes determine the topology selected for a specific converter. The functions of a power converter include:

- Isolation from the Powerline
- Meet Powerline Standards
- Provide regulated dc Voltage(s)
- Power Sequencing and Control

1.2 Up Vs. Down Conversion

One primary explanation between various topologies is whether the output voltage of the converter is above or below the input supply voltage. If the output voltage is lower than the input voltage it is referred to as 'down conversion'. If the output voltage is higher than the input voltage it is referred to as 'up conversion'. Up conversion is sometimes referred to in the literature as 'boost' and down conversion as 'buck'. Often the two terms can be used interchangeably, but it should be noted that 'boost' and 'buck' are also the names of much more specific dc/dc converter topologies. For that reason, we will use 'up conversion' and 'down conversion' when referring to the voltage transformation through the converter in the more general sense. Both of these techniques find prevalent use in electronic equipment, some examples of which are listed below

Common applications of up conversion

- Power Factor Correction (PFC)
- Generation of higher voltages in battery powered equipment
- Generation of backlight voltages for LCD displays
- UPS systems

Common applications of down conversion

- Most dc/dc power modules
- Most ac/dc converters
- IC Linear regulators

1.3 Literature Review

The technical literatures contributed by esteemed authors and scientists that have been reviewed for this thesis work is quoted here along their works carried out by their own:

According to Vorperian, V 'c and Zeljko Mrcarica Power electronic components (transistors, thyristors, and diodes) for convenience are often modeled as switches. Instances of such models may be found in switched capacitor or switched-current networks, switched power supplies, mixed signal circuits such as A/D converters, etc. The advantage of using ideal switches in circuit simulation is explained. To simplify, if nonideal models are used in a SPICE-like simulation, simulation of the resulting stiff system demands long simulation times. When switches are modeled as ideal, simulation for the switch transition is performed in one time instant, rather then as a step transition of voltages and currents.

Yao, K.; Meng, Y; Lee, F. proposed a Power factor correction achieved by using discontinuous current regime. With all the disadvantages this regime is introducing (higher current peak values through semiconductor devices and the voltage drop across them), using this regime a power factor almost equal to unity can be obtained. This method was implemented in a SEPIC converter, the theoretical results obtained from Pspice and Matlab simulations being verified on the experimental converter.

Jacek J. Jozwik and Marian k. Kazimierczuk presented a steady-state analysis an experimental result for a dual sepic PWM dc/dc power converter for the continuous

and discontinuous modes of operation. The converter is dual to a sepic converter, but it can also be derived from a forward converter by replacing one of its rectifier diodes with a coupling capacitor. The circuit acts as a step-down or step-up

converters depending on the value of the ON switch duty cycle. The transformer less version of the converter has a Positive dc/dc voltage transfer function. Therefore, the circuit is suitable for distributed power systems. Design equations are derived for all circuit Components. Experimental results measured at 100 kHz were in good Agreement with the theoretical predictions.

K. O. Gusseme, O. Van de Sype, A proposed a high efficiency active clamp sepic-flyback converter. The proposed converter is superposition of sepic converter mode and flyback converter mode. Not only sepic mode output but also flyback mode output can be fully regulated by constant frequency PWM control. Merging sepic and flyback topology can share the transformer, power MOSFET, and active clamp circuit. It has outstanding advantages over the conventional dc-dc converters with respect to high efficiency, high power density, and component utilization. The operation principle of the proposed converter is described and verified by simulation and experimental results.

J Knight, S. Shirsavar and WHolderbaum (2010) suggested that how we can obtain a nonisolated high step-up converter with the arrangement of a boost converter with a series output module. A boost inductor and a switch are shared by the boost and the SEPIC converter therefore its structure is simple. The current snubber is not required for the diodes in the SIB converter because the transformer leakage inductor alleviates the reverse recovery.

S. Dwari and L. Parsa, proposed a continuous-conduction-mode SEPIC converter for power factor correction with low reverse-recovery loss . The proposed

SEPIC converter can reduce the reverse recovery loss of the diodes and improve the power efficiency. By utilizing a coupled inductor and an additional diode, zero-current turn-off of the output diode is achieved. The reverse-recovery

current of the additional diode is reduced by the leakage inductor of the coupled inductor. The proposed SEPIC converter provides high power efficiency and high power factor compared to the conventional PFC circuits employing the SEPIC converter. An operation principle and a detailed analysis of the proposed converter are presented. Experimental results show that the efficiency of the SEPIC converter can be significantly improved.

C. L. Shen, Y. E. Wu and M. H. Chen presented A dc-dc converter is capable of operating in both step-up or stepdown mode and widely used in battery-operated equipment. There are two possible modes of operation in the SEPIC converter: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). This paper presents modeling of a SEPIC converter operating in CCM using the State-Space Averaging (SSA) technique. The modeling leads to a small-signal linear model of the converter, from which the transfer functions used for feedback control design can be determined. Results are presented to verify the accuracy of the obtained model.

Domingos S'avio Lyrio Simonetti, Member, IEEE, Javier Sebasti presented a paper for an interleaved sepic converter with low turn-on switching loss is. Power switches can be turned on with zero-voltage-switching (ZVS) feature when it is operated at duty cycle greater than 0.5. Although, the proposed converter is operated at hard switching when the duty cycle is less than 0.5, the smooth current by the resonant inductance can reduce the turn-on switching loss. Thus the total switching losses can be reduced compared to the hard switching converter. The interleaved PWM scheme can also reduce the current ripple at the input and output capacitors. Thus the size of inductor and capacitor can be reduced.

Esam H. Ismail, Senior Member, IEEE and Abbas A. Fardoun proposed an improved version of a SEPIC converter consists of a conventional SEPIC

converter plus an additional high-frequency transformer and diode to maintain a freewheeling mode of the dc inductor currents during the switch on state. The voltage conversion ratio characteristics and semiconductor device voltage and current stresses are characterized. The main advantages of this converter are the continuous output current, smaller output voltage ripple, and lower semiconductors current stress compared with the conventional SEPIC converter.

Mr. R. B. Darla (2007) analyzed the Photovoltaic module and SEPIC converter characteristics. The technique is based on linking a pulse width modulated dc-dc SEPIC system, which is controlled by a micro controller based unit. The main difference between the method used in the proposed system and other method used in the past is that Photovoltaic panel output power is used to directly control the dc-dc converter thus reducing the complicatedness of the system.

Mukhtar Ali, Mohamed Orabi, Mahrous E. Ahmed and Abdelali El-Aroudi, (2010) deals with the application of SEPIC converter as a driver for Light emitting Diode lighting system. The advanced SEPIC converter has recognized by its improvement for lower voltage stresses. The advanced SEPIC converter differs in two ways Compared to the conventional SEPIC converter. The capacitor C_1 is a large bulk capacitor and a diode is placed in series with the inductor L_2.

V. von Kaenel, P. Macken, and M. G. R. Degrauwe (2008) introduced a current-shaper SEPIC converter for high brightness LEDs is introduced. It is for the high brightness LED lighting applications with universal input voltages proposing a high power factor SEPIC converter. The converter operates in discontinuous conduction mode. Because of the input inductor current which follows the input voltage harmonics of the input line current is reduced and power factor is improved.

Roberto F. Coelho, Filipe M. Concer, Denizar C. Martins discussed about the analysis and control of two-input buck integrated SEPIC converter which is appropriate for Photovoltaic (PV) applications. This proposed converter is fundamentally combination of individual buck and SEPIC converters. The SEPIC converter with maximum power tracking take outs complete power from the Photovoltaic array and feeds into the load.

S. M. Ćuk and R. D. Middlebrook Chung (2005) presented a high efficiency active clamp SEPIC-flyback converter. The modified converter is superposition of SEPIC converter mode and flyback converter mode. It has exceptional advantages over the conventional dc-dc converters regarding high power density, high efficiency and component utilization.

1.4 Thesis Objectives

The Managerial literatures contributed by that are quoted here along their works carried out their own:

- How SEPIC is useful in solar power system
- How SEPIC improves the quality of the Solar power
- How to implement SEPIC in Transmission and distribution of power
- How to reduce the power loss by using SEPIC converter

1.5 Thesis Organization

This dissertation is organized in five chapters. Each chapter is described along with necessary theory required to comprehend it.

Introduction about the need of dc-dc converters is given in chapter 1 which indicates that how a dc-dc converter works. It presents an historical review of the dc-dc conversion and summarizes with the application of dc-dc converter in present era.

Explanation about different dc - dc converters has been discussed in chapter 2. It initiates with the presentation of different types of dc-dc converters such as Buck, Boost, Buck-Boost and Cuk converters. Switching and conduction losses in hard switched converters are described here. At the end of this chapter, control scheme and noise reduction by filtering are explained under resonant converter category.

The designing and analysis of SEPIC topology based dc-dc converter is presented in chapter 3. Here we studied that how a SEPIC converter operates. Duty cycle and selection of different components for SEPIC converter are also explained. Further derivation of the model equation for SEPIC system is given here. Critical conduction parameters have been also discussed. We have deliberated about the designing of inductors L_1, L_2 and intermediate capacitor C_1. Finally this chapter explained about various control strategy.

The modified converter circuits are simulated using MATLAB software in chapter 4. Voltage and current Wave forms of different circuit elements are drawn.

CHAPTER 2

Dc-Dc Conversion Principles

In this chapter, the principles used in dc-dc conversion are explained. In the first part, the most popular type of voltage converters is presented: the linear regulator. In the second part, the switching converters are described and analyzed. Finally, in the third part, the controllers used in the switching converters are exposed and their different regulation principles are explained.

Each electronic power converter consists in a power processor, a controller, and a voltage reference. The input power coming from the supply is converted by the power processor and provided to the load. The power processor can be a current, a voltage, or a frequency converter (or any combination of these physical quantities). It consists of power electronic devices like mosfet, diode, thyristors etc. The feedback controller compares the output voltage of the power processor with a reference voltage value, and acts on the power processor so that the error between the two is minimized. Both linear regulators and switching regulators use this elementary regulation principle.

2.1 Classical Type Dc/Dc Converter

Figure 2.1 shows the classical, or Royer, type dc/dc converter circuit. The transistor switches operate in a push-pull configuration with a center-tapped transformer. When input voltage is first applied to the circuit, one of the transistor switches begins to turn on. The transformer provides positive feedback to the base of this transistor, turning it on hard. This switch remains on until the

magnetic flux of the transformer saturates, causing the transformer voltage to reverse, thereby turning off the first transistor and turning on the second one.

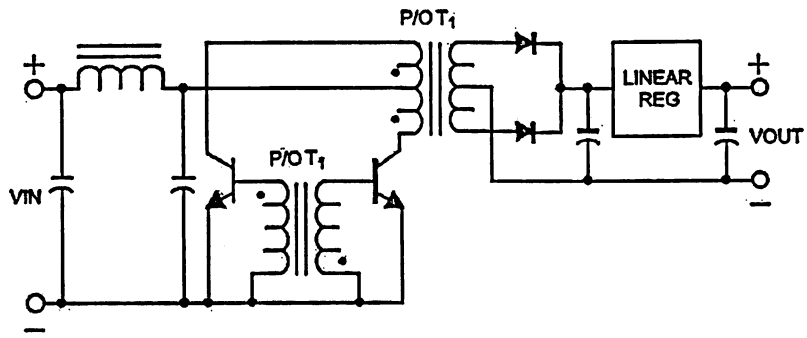

Fig2.1 Classical Dc- Dc Converter

The circuit continues to self-oscillate and produces an output square wave of voltage which is full-wave rectified and filtered. This rectified square wave, before filtering, appears as show in Figure 2.2, since the square wave is of high frequency, with a relatively fast rise and fall time; it is relatively easy to filter with an electrolytic capacitor.

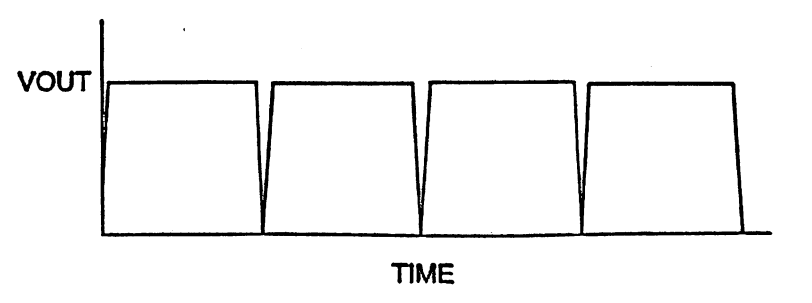

Fig 2.2 Converter Output Voltage after Rectification

The rectified and filtered square wave, however, is not regulated, and any change in input voltage will be transferred directly to the output. Regulation is provided by a linear output regulator which gives a constant dc output voltage and also provides current-limiting and short circuit protection on the output.

The classical dc/dc converter is widely used today, provider economical dc voltage conversion. Since the regulation is dissipative in this converter, overall efficiency is generally limited to about 65%. As in the linear power supply, the linear regulator must operate with sufficient voltage drop across the series pass element at the minimum input voltage the converter. This establishes one operating point. As input voltage increases, the drop across the series passes element and the dissipation increase directly. Therefore, to maintain reasonable efficiency, the input voltage range is usually ±10% with some units as wide as -12% to +30%.

2.2 Switching Voltage Converters

A popular type of dc/dc converter is the switching regulator shown in Figure 2.3. This is a three-terminal, non-isolated circuit which converts a higher dc voltage into a lower one with a typically wide range input voltage; the input voltage range may be as high as 4 to 1. With this type converter, output power levels to 300 watts are achievable.

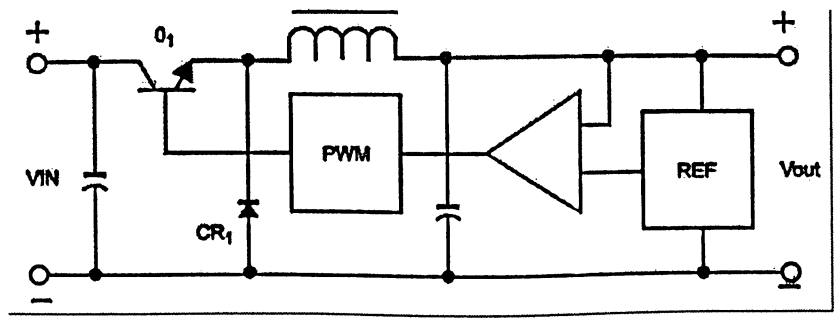

Fig2.3 Three Terminal Dc/Dc Converter

The output voltage is compared with a reference voltage and the difference is amplified to drive a pulse-width modulator which in turn drives the switch. The energy stored in the inductor is determined by the on-time to off-time of the switch. Current flows through the inductor during both halves of the switching cycle, either through Q1 or through CR1.

Switching regulators generally use an oscillator for generating a clock signal, active elements as switches, and reactive passive elements (like capacitive and magnetic devices) for storing the energy to convert. If the switching elements are considered without their parasitic, the efficiency of switching converters can theoretically reach 100%. Practically, unlike linear regulators in which the pass-device is used as an adjustable resistor, in switching converters only the parasitic lower the power conversion efficiency.

There are two main types of switching regulators. The simplest one is made only with capacitive components and switching devices: it is called switched capacitor converter. It is also often called inductor-less converter or charge pump. This type of converter is mainly used in integrated circuits to multiply or divide the power supply voltage with a higher efficiency than a linear regulator. Charge pumps are generally low power converters using MOSFETs as active switching elements.

A more flexible and powerful type of switching regulator is the dc-dc converter using both capacitive and magnetic passive devices, in combination with active switching devices. The capacitive devices are integrated or discrete capacitors, while the magnetic devices are generally discrete power inductors or power transformers. Different active devices are used to design such converters, depending on the application's needs. These devices are mostly transistors, diodes and thyristors.

2.3 Switched Capacitor Converters

While the classic dc-dc converters use capacitors and inductors (see Section 2.1), the switched capacitor converters are only designed with capacitors. Switched capacitor dc-dc converters are low power converters that consist of power switches and energy transfer capacitors in the power stage. The switches are periodically turned on and off, so that the converter cycles through a number of switched networks. These topologies are not adapted to high power converters. Because they make no use of inductors, these converters can be completely integrated into a single silicon chip (power inductors are difficult to integrate on silicon). There is no need to use neither off-chip capacitors nor inductors. The output power in the target applications is in the mill-watt range. The silicon area occupied by the converter and its on-chip capacitors can be very important. Most of the silicon area used by the switched capacitor converter is occupied by the MOS capacitors constituting the switched capacitor network. However, in deep sub-micron mixed-signal technologies, metal-metal capacitors (MMC) are the best choice. They provide a lower equivalent series resistor (ESR) and higher breakdown voltages, thus reaching a higher efficiency.

A major advantage of the switched capacitor converters is that they eliminate the magnetic fields and EMI that comes with an inductor or a transformer. A drawback is that they do not provide high conversion efficiency if the needed voltage conversion factor is not an integer.

The circuit shown in Figure 2.4 represents a basic switched capacitors no inverting voltage doubler. During operation, two states of equal duration occur. During the first state, the capacitor C1 is charged with the input voltage Vin through the switches T1 and T2 (T3 and T4 are open). During the second state, T3 and T4 are closed, while T1 and T2 are open. The voltage across C1 (i.e., the

voltage Vin at which C1 has been charged during the first state) is added to the input voltage Vin, and provided to the output filter capacitor Cout. Therefore, the voltage Vout provided to the output is two times the input voltage Vin. Thus, the voltage conversion ratio M of this circuit is given by:

$$M = \frac{V_{out}}{V_{in}} = 2 \qquad (2.1)$$

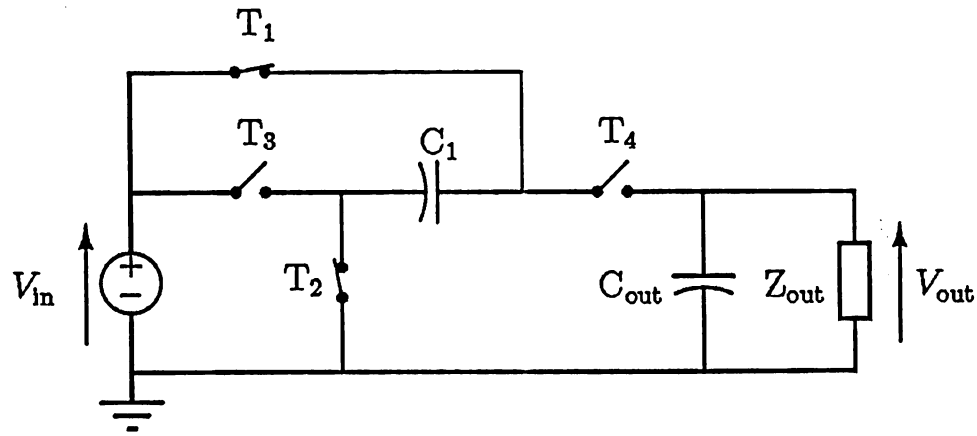

Figure 2.4 Schematic of a voltage doubler with switched capacitors

2.4 Basic dc-dc Converter Topologies

In the following approaches, the converters are supposed to operate in steady-state with a constant input voltage Vin and a constant output voltage Vout. Further, the components used in the power paths are taken ideal and no parasitics

are considered (e.g., the power transistors are assimilated to ideal switches having an infinite resistance when turned off, and no resistance when turned on). However, the parasitic in the power paths are analyzed and discussed in detail by the precise component models used in advanced circuit simulations.

The basic circuits used to design advanced dc-dc converters consist in three main topologies, which are the step-down topologies (like the buck converter shown in Figure 2.4), the step-up topologies, and the topologies able to perform both step-up and step-down conversion. Some circuits are also able to perform polarity inverting at output (e.g., converting an input voltage of 3.3V into a negative output voltage of −5 V). The step-down topologies are only able to provide an output voltage lower than the input voltage, while the step-up topologies are only able to provide an output voltage higher than the input voltage. The combination of a step-up and a step-down topology enables both voltage reduction and voltage increase with a single switching converter.

The energy storage devices (i.e., capacitors, inductors or transformers) are the heart of any switching-mode power supply. Switching regulators use inductors which are usually wound on steroidal cores, often made of ferrite or powdered iron core with distributed air-gap to minimize core losses at high frequencies. Transformers are mostly used in isolated topologies. However, in this research work, only nonisolated topologies using capacitors and inductors are considered, because transformers are not easily inferable in mobile systems.

A capacitor stores its energy in an electrical field. This field builds up when a voltage VC1 is applied to the capacitor's terminals. The ability of a capacitor to store energy in the form of an electric field, and consequently to oppose changes in voltage, is called capacitance. The capacitor equation states that the current IC1 flowing through the capacitor C1 is proportional to the rate of change in

voltage VC1 at the capacitor's terminals. The constant of proportionality is the capacitance C1.

2.4.1 Buck Converter

The buck converter is used for step down operation. A buck converter with its output filter arrangement is as shown in figure 2.5.

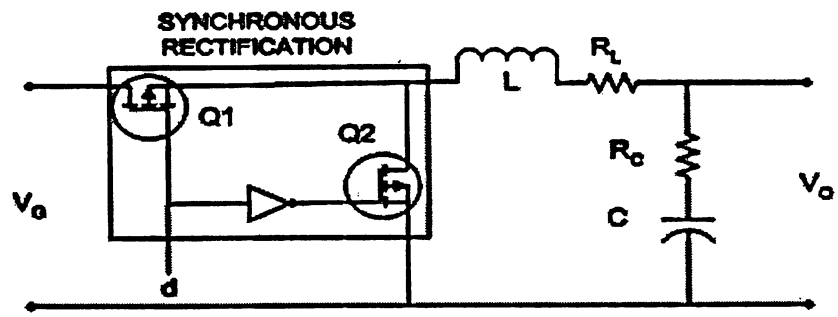

Figure 2.5 Buck Converter

When the transistor Q1 is on and Q2 is off, the input voltage appears across the inductor and current in inductor increases linearly. In the same cycle the capacitor is charged. When the transistor Q2 is on and Q1 reversed. However, current in the inductor cannot change instantaneously and the current starts decreasing linearly. In this cycle also the capacitor is also charged with the energy stored in the inductor is off, the voltage across the inductor is reversed. However, current in the inductor cannot change instantaneously and the current starts decreasing linearly. In this cycle also the capacitor is also charged with the energy stored in the inductor.

There is the possibility of two modes of operation namely continuous and discontinuous mode. In continuous mode, the inductor current never reaches zero and in discontinuous mode the inductor current reaches zero in one switching cycle. At lighter load currents the converter operates in discontinuous mode. The regulated output voltage in discontinuous mode no longer has a linear relationship with the input voltage as in continuous conduction mode operation.

2.4.1.1 Synchronous rectification

The transistor Q2 is used instead of a diode for higher efficiency. This is synchronous rectification. The forward voltage drop across a diode during the second cycle is appreciable and reduces the converter efficiency. To the contrary in a well designed circuit transistor voltage is much less than the forward diode voltages drop. However, synchronous rectification requires non-overlap logic to avoid supply shunt currents which results when both transistors are on.

2.4.1.2 Inductor Volt-Second Balance

Analyzing the inductor current waveform determines the relationship between output and input voltage in terms of duty cycle. In a well designed converter, the main objective is to have small percentage of ripple at the output. As a result, the output voltage can be approximated by its dc component. Inductor current is found by integrating the inductor voltage waveform. Inductor voltage and current waveforms for a buck converter are as shown in figure 2.6.

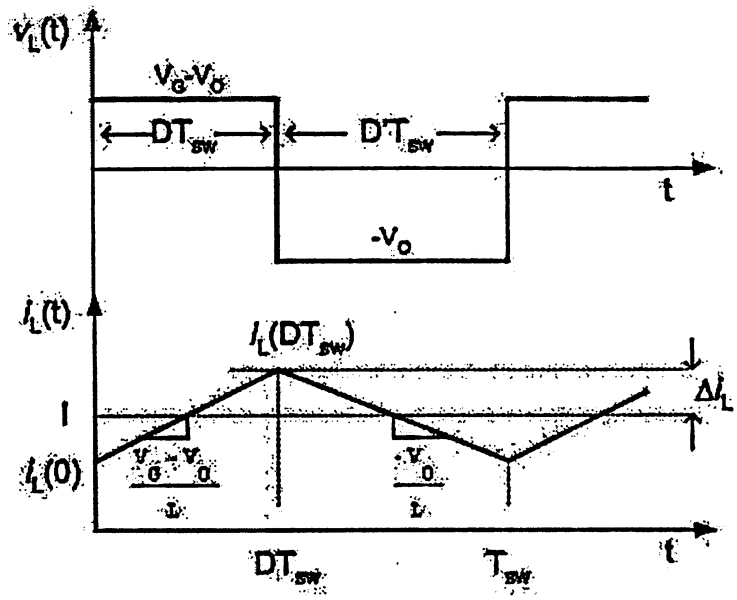

Figure 2.6 Steady-state inductor voltage and current waveform

In steady state, the observation that over one switching period the net change in inductor current is zero is the principle of inductor volt second balance. The inductor voltage definition is given by equation (2.2).

$$vl(t) = l\, dil/dt \qquad (2.2)$$

Integration over one complete switching period yields,

$$\int_0^{sw} \mathrm{vl(t)dt} \qquad (2.3)$$

The left hand side of above equation is zero. As a result (2.2) can be written as;

$$\int_0^{sw} vl(t)dt = 0 \qquad (2.4)$$

The equation 2.3 has the unit of volt-seconds or flux-linkages. Alternatively, total area under the *V*l(t) waveform over one switching period must be zero. Area under the *V*l(t) curve is given by

$$A = \int_0^{Tsw} Vl(t)dt = (Vg - Vo(DTsw) + (-Vo(DTsw) \qquad (2.5)$$

Average value of inductor voltage is given by,

$$(Vl) = \frac{A}{Tsw} = D(Vg - Vo) + D(-Vo) \qquad (2.6)$$

By equating *L v* to zero and using relation d+d = 1, and solving for Vout yields

$$Vo = D.Vg \qquad (2.7)$$

2.4.1.3 Capacitor Charge Balance

Similar to the inductor volt-second balance, the defining equation for capacitors is

$$ic(t) = C\frac{dVc(t)}{dt} \qquad (2.8)$$

Integration over one complete switching period yields,

$$vc(Tsw) - vc(0) = \frac{1}{C}\int_0^{sw} 1c(t)dt \qquad (2.9)$$

In steady state, the net change over one switching period of the capacitor voltage must be zero, so that the left hand side of the above equation is zero. Equivalently stated the average value or the dc component of the capacitor must be zero at equilibrium.

$$(ic) = \frac{1}{Tsw}\int_0^{sw} 1c(t)dt = 0 \qquad (2.10)$$

Thus the principle of capacitor charge balance can be used to find the steady state currents in a switching converter.

2.4.2 Boost Converter

The boost converter is capable of producing a dc output voltage greater in magnitude than the dc input voltage. The circuit topology for a boost converter is as shown in figure 2.7.

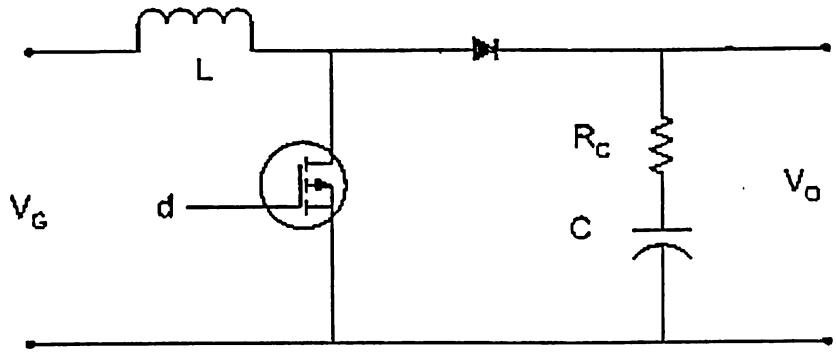

Figure 2.7 Boost Converter

When the transistor Q1 is on the current in inductor L, rises linearly and at this time capacitor C, supplies the load current, and it is partially discharged. During the second interval when transistor Q1 is off, the diode D1 is on and the inductor L supplies the load and, additionally, recharges the capacitor C. The steady state inductor current and voltage waveform is shown in figure 2.8.

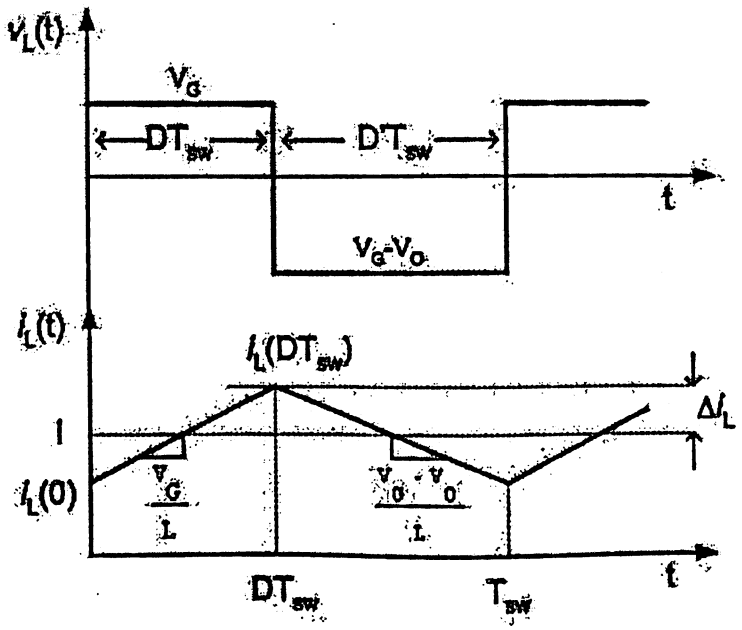

Figure 2.8 Steady-state inductor voltage and current waveform

Using the inductor volt balance principle to get the steady state output voltage equation Yields

$$Vg.Ton + (Vg - Vo).Toff = 0 \qquad (2.11)$$

$$\frac{Vo}{Vg} = \frac{Tsw}{Toff} = \frac{1}{1-D} \qquad (2.12)$$

Since the converter output voltage is greater than the input voltage, the input current which is also the inductor current is greater than output current. In practice the inductor current flowing through, semiconductors Q1 and D1, the inductor winding resistance becomes very large and with the result being that component non-idealities may lead to large power loss. As the duty cycle approaches one, the inductor current becomes very large and these components no idealities lead to large power losses. Consequently, the efficiency of the boost converter decreases rapidly at high duty cycles.

2.4.3 Buck-Boost Converter

The buck-boost converter is capable of producing a dc output voltage which is either greater or smaller in magnitude than the dc input voltage. The arrangement for the buck-boost converter is as shown in figure 2.9.

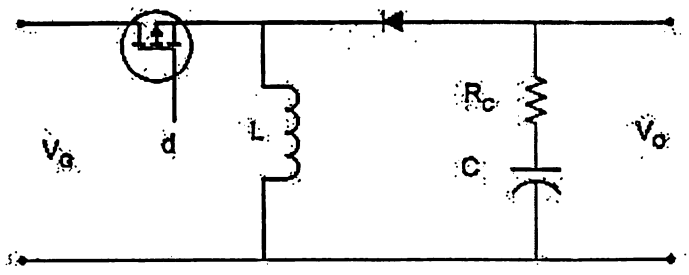

Figure 2.9 Buck-boost converter

When the transistor Q1 is on, input voltage is applied across the inductor and the current in inductor L rises linearly. At this time the capacitor C, supplies the load current, and it is partially discharged. During the second interval when the transistor is off, the voltage across the inductor reverses in polarity and the diode conducts. During this interval the energy stored in the inductor supplies the load and, additionally, recharges the capacitor. The steady state inductor current and voltage waveform is shown in figure 2.10.

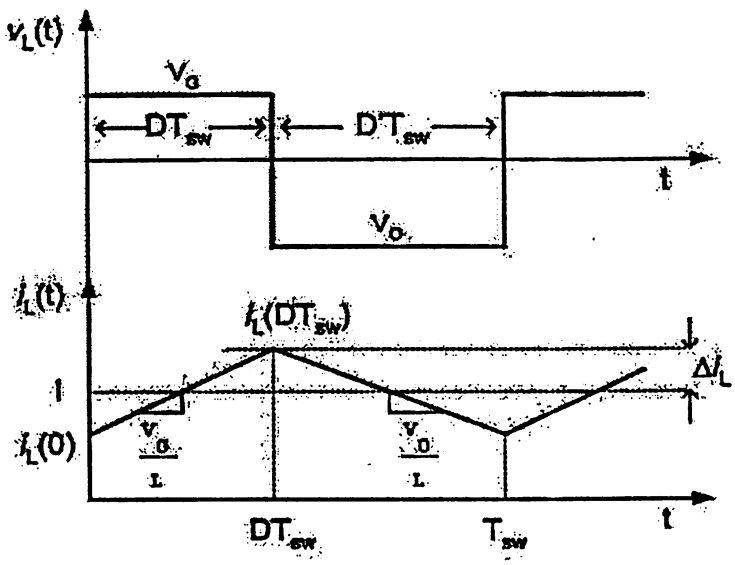

Figure 2.10 Steady-state inductor voltage and current waveform

Using the inductor volt balance principle to find the steady state output voltage equation Yields;

$$Vg.Ton = Vo.Toff = 0 \qquad (2.13)$$

$$\frac{Vo}{Vg} = \frac{Tsw}{Toff} = \frac{D}{1-D} \qquad (2.14)$$

The D varies between 0 and 1 and thus output voltage can be lower or higher than the input voltage in magnitude but opposite in polarity.

The conversion ratio M buck- boost (inv) can vary between minus infinity and 0 (i.e., M buck-boost (inv) $\in [-\infty, 0]$). This means that the buck-boost converter provides a negative voltage at its output. This converter has a high input and a high

output current ripple due to the inductor alternatively placed on the input and the output. Figure 2.11 shows the absolute value of the transfer functions of the buck, buck-boost, and boost converters.

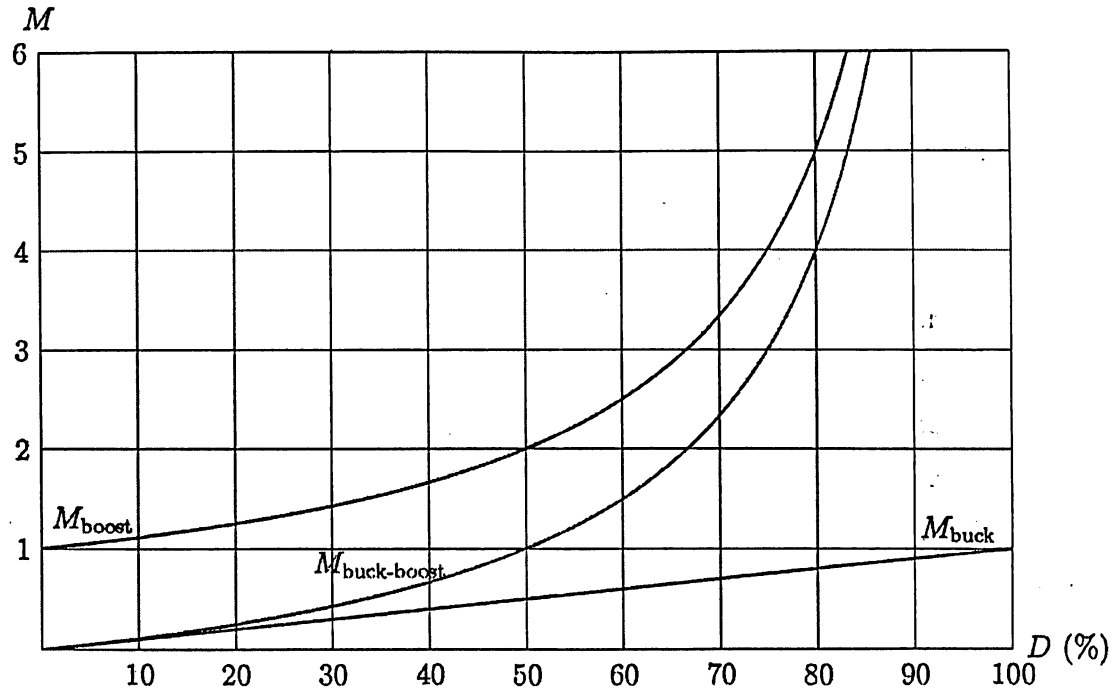

Figure 2.11 Buck, Buck-boost, and Boost transfer functions in CCM

2.4.4 Cuk Converter

The Ćuk converter shown in Figure 2.12 can either increase or decrease the input voltage Vin. It also inverts the polarity, like the inverting buck-boost converter. The Ćuk converter operates via capacitive energy transfer. When M_1 is turned on, the diode D_1 is reverse biased, the current in both L_1 and L_2 increases, and the power is delivered to the load. When M_1 is turned off, D_1 becomes forward biased and the capacitor C_1 is recharged.

To determine the relation between V_{in} and V_{out}, two states must be considered:

• State 1: M_1 is turned on, D_1 is reverse biased ($0 < t < t_{on}$):

:

$$V_{L1} = Vin \qquad (2.15)$$

$$V_{L2} = Vout + V_{C1} \qquad (2.16)$$

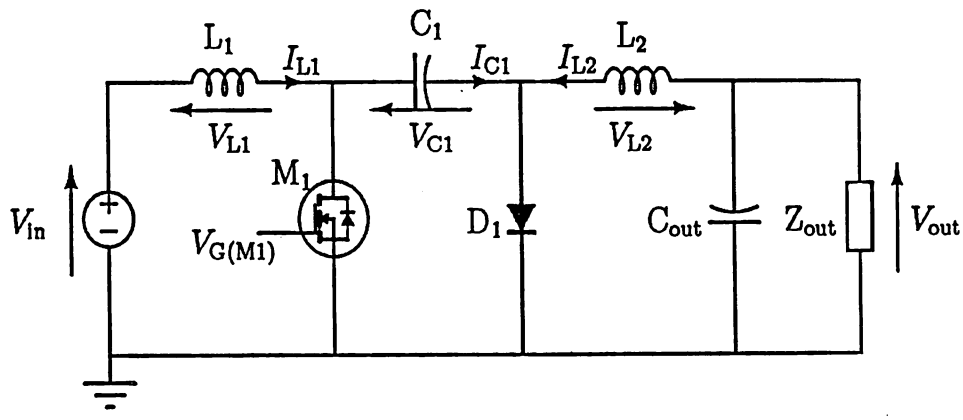

Figure 2.12 Ćuk converter schematic

• State 2: M_1 is turned off, D_1 is forward biased ($ton < t < t_{sw}$):

:

$$V_{L1} = Vin - V_{C1} \qquad (2.17)$$

$$V_{L2} = Vout \qquad (2.18)$$

When the converter performs in the steady-state, the capacity C1 is supposed to be large enough so that the voltage ripple across C1 can be neglected. Thus, VL1 and VL2 are also constant between [0, ton[and]ton, tsw] with a discontinuity step at t = ton. The inductor current change through L2 during steady-state operation expressed in Equation is therefore written:

$$\int_0^{t_{on}} V_{L2} \cdot dt + \int_{t_{on}}^{t_{sw}} V_{L2} \cdot dt = 0 \qquad (2.19)$$

By replacing VL2 in Equation (2.19) with the expressions from Equation (2.17) and Equation (2.18), it is obtained:

$$\int_0^{t_{on}} (V_{out} + V_{C1}) \cdot dt + \int_{t_{on}}^{t_{sw}} V_{out} \cdot dt = 0 \qquad (2.20)$$

Integrating Equation (2.20) yields:

$$(V_{out} + V_{c1}) \cdot (t_{on} - 0) + V_{out} \cdot (t_{sw} - t_{on}) = 0 \qquad (2.21)$$

$$V_{c1} = -V_{out} \cdot \frac{t_{sw}}{t_{on}} \qquad (2.22)$$

The steady-state current change through L_1 is expressed by:

$$\int_0^{t_{on}} v_{L1}.dt + \int_{t_{on}}^{t_{sw}} V_{L1}.dt = 0 \tag{2.23}$$

By replacing V_{L1} in Equation (2.23) with the expressions from Equation (2.17) and Equation (2.18), it is obtained:

$$\int_0^{t_{on}} V_{in}.dt + \int_{t_{on}}^{t_{sw}} (V_{in} - V_{c1}).dt = 0 \tag{2.24}$$

Integrating Equation (2.24) yields:

$$V_{in}.(t_{on} - 0) + (V_{in} - V_{C1}).(t_{sw} - t_{on}) = 0 \tag{2.25}$$

$$V_{in}.(t_{on} - 0) + \left(V_{in} + V_{out}.\frac{t_{sw}}{t_{on}}\right).(t_{sw} - t_{on}) = 0 \tag{2.26}$$

$$V_{in}.t_{sw} + V_{out}.\frac{t_{sw}}{t_{on}}.(t_{sw} - t_{on}) = 0 \tag{2.27}$$

Finally, the voltage conversion ratio $M_{Ćuk}$ of the Ćuk converter is given by:

$$M = \frac{V_{out}}{V_{in}} = \frac{-t_{on}}{t_{sw} - t_{on}} = \frac{-D}{1 - D} \tag{2.28}$$

The conversion ratio $M_{Ćuk}$ can vary between minus infinity and 0. The Ćuk topology has the inductor L_1 always connected to the input and the inductor L_2 always connected to the output, thus providing low input and output current ripples. The Ćuk converter can be made a bidirectional converter by replacing the diode D_1 through a power mosfet. The drawback of the Ćuk converter is the need of two power inductors (i.e., L_1 and L_2) and an additional capacitor for the energy transfer (i.e., C_1).

2.4.5 Zeta Converter

The zeta converter shown in Figure 2.13 is build by interchanging the transistor M1 and the diode D1 from the SEPIC topology, and by also interchanging the I/O power terminals. Thus, it is also known as the inverse of SEPIC converter. The operating principle of the zeta converter is comparable to the SEPIC converter. At the beginning of each switching period, the energizing transistor M1 is turned on and the current through the inductor L1 increases. During this phase, the diode D1 is reverse biased and the energy stored in the capacitor C1 makes the current through the inductor L2 to increase (i.e., energy is transferred to the output). When M1 is turned off, the current in the inductor L1 forces D1 to turn on. The energy stored in the inductor L1 is transferred to the capacitor C1 and the current through the inductor L2 decreases.

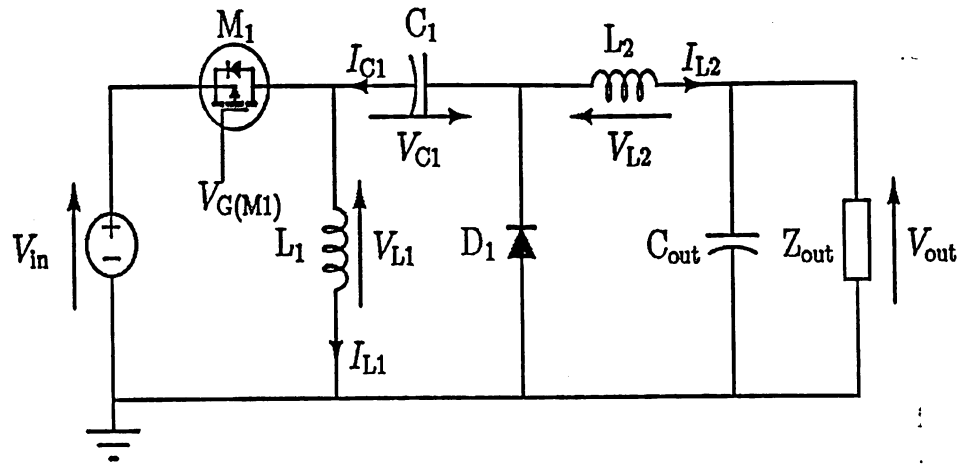

Figure 2.13 Zeta converter schematic

By using the same methodology as for the Ćuk converter in Section 2.4.4, the voltage conversion ratio M_{zeta} of the zeta converter is given by:

$$M_{zeta} = \frac{V_{out}}{V_{in}} = \frac{t_{on}}{t_{sw} - t_{on}} = \frac{D}{1 - D} \tag{2.29}$$

The conversion ratio M zeta can vary between 0 and infinity. The zeta topology has the inductor L_2 always connected to the output, thus providing low output current ripple. Since there is no inductor always connected to the input, this topology provides high input current ripple.

2.5 Isolated dc-dc converter

2.5.1 Transformer Isolation

The use of a transformer allows dc isolation and multiple outputs in a dc-dc converter. Since the transformer size and weight vary inversely with frequency, significant improvements can be made by incorporating the transformer into the converter. Through a proper choice of transformer turns ratio and switching frequency stresses imposed on the transistors and diodes can be minimized. This leads to improved efficiency at lower cost. Multiple dc outputs are obtained by adding multiple secondary windings and converter secondary side circuits. The secondary turns ratios are appropriately chosen to get the desired output voltages.

2.5.2 Flyback Converter

Figure 2.14 shows the Flyback converter. When the transistor Q1 is turned on, the energy is stored in the power transformer while the load current is supplied from output capacitor C. When the transistor is turned off, the energy stored in transformer is transferred to output as load current and to recharge the capacitor.

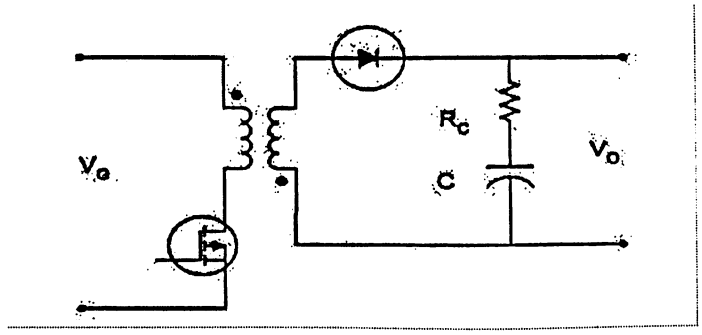

Figure 2.14 Flyback converter

One of the major advantages of Flyback converter is that they don't require an output filter inductor, thus saving cost and volume. This also makes Flyback converters valuable for high output voltages unlike forward converters which have an output inductor potentially causing problems as the inductor must sustain large voltages. Flyback also doesn't require a high voltage freewheeling diode. The filter capacitor at the output is typically larger in Flyback converters as it alone supplies the load current when the transistor is ON. Equivalently the full dc current flows from ground through the capacitor to the load during the transistor ON time. Thus the ripple current rating of the capacitor and output ripple voltage requirement collectively determines the final choice of output filter capacitor.

2.6 Switching Controllers Considerations

In a switching converter (e.g., in the buck converter), the controller pilots the power devices, and therefore acts directly on the power conversion efficiency. Several tasks are accomplished by the controller. One of them consists of protecting the power devices against destructive effects (e.g., overcurrent, temperature overstress) by monitoring the currents, the voltages, and the temperature. However, its principal role is to regulate the output voltage V_{out} to the requested voltage value. To do this, the controller can be designed to use different operation control methods, each of them adapted to a specific case. These operation control methods are discussed in this Section. The two most popular regulation principles are voltage mode and current mode.

2.6.1 Operation Control

Mainly two different modulations are used in today's dc-dc converters, each optimized for a specific load condition (i.e., a different output power range). The first is the pulse-width modulation (PWM) operation control method, which is well suited for high power conversions. The second is the pulse-frequency modulation (PFM) operation control method, which is better suited for low power conversions. By combining both of these operation control methods into one controller, the converter can be made very efficient over a wide range of output power.

2.6.2 Pulse-Width Modulation Control

With the pulse-width modulation control, the regulation of output voltage is achieved by varying the duty cycle D of the switching devices, keeping the frequency of operation constant. Usually, the operation control by pulse-width modulation is the preferred method, since constant frequency operation greatly simplifies the design of the regulation feedback loop and the output ripple filter, thus avoiding stability issues. However, since the switching frequency is constant in the PWM control scheme, the switching losses (e.g., the losses due to the charging/discharging of the gate and output capacitances of the power transistors) are independent of the load current. The direct consequence is that PWM becomes inefficient when a light load is supplied, because the switching losses dominate the conduction losses, which are load dependent.

2.6.3 Pulse-Frequency Modulation

To overcome the dramatic efficiency reduction in lightly loaded PWM converters, an additional operation control scheme called pulse-frequency modulation (PFM) has been developed. PFM is a nonlinear operation scheme in

which pulse trains are applied to the energizing switch to maintain the output voltage within the preset voltage range. This mode lowers the frequency of the switching-cycle events, therefore lowering the switching losses, which are dominant to the

conduction losses at light output loads (i.e., when the requested output current is low). Although PFM control has become prevalent in battery-operated mobile equipment because its light-load efficiency exceeds that of PWM, PFM is more difficult to design because this operation control scheme has some important issues concerning the stability in the frequency domain, since it is a variable-frequency control scheme. PFM allows to extend battery life of the mobile equipment in the suspend and standby modes of operation. However, the low frequencies can cause switching noise to enter the audio band. This can be avoided by sizing the passives so that the PFM converter is forced to operate above the audio band at the minimum load condition.

There are several PFM operation schemes, such as single-pulse PFM, multi-pulse PFM, and burst-mode PFM. However, all operate according to the basic principle of initiating switching cycles only as needed to maintain the output voltage. Figure 2.15 shows the waveforms produced by a burst-mode PFM controller. The pulse trains represent the PFM operation control. The ripple on the output voltage Vout has been increased for readability reason. In practice, this voltage ripple does not exceed 150mV peak-to-peak voltage.

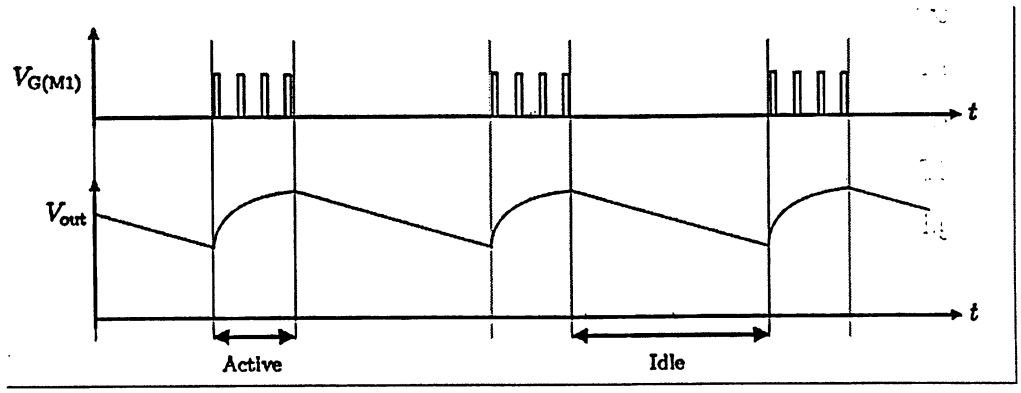

Figure 2.15 Signal waveforms of the PFM control in steady-state.

In dc-dc converters for mobile equipment, the PFM operation control is never used standalone. It is always coupled to a PWM controller. The current trend in today's dc-dc converters is to increase the switching frequency of the controllers, so that the passive device sizes (i.e., inductors and capacitors) can be reduced. To enable future on-chip hybrid integration of power inductors, the switching frequencies are approaching 10MHz and they will continue to increase. Therefore, the most efficient way to reach high efficiency in both heavy and light load conditions is to combine both PWM and PFM operation control schemes.

2.7 Dc-To-Dc Converter Noise Reductions

The inherent switching inside the dc-to-dc converter gives rise to potential sources of noise. This noise manifests itself on the output voltage as spikes at the switching frequency. Due to size and cost requirements, internal filtering is limited but usually adequate for most applications. When excessive noise is suspected, you must rule out extraneous noise sources. If the circuit requires less noise than the supply is capable of, there are two preferred filter techniques—LC filters or an output filter capacitor.

2.7.1 LC Filtering

For applications requiring higher accuracy, such as analog measurements, LC filters should be used on each channel to attenuate high-frequency noise. Because of the output filter capacitor already present in the dc-to-dc converter, adding an inductor and capacitor to the output creates a PI filter at half the use-capacitor cost (Figure2.16).

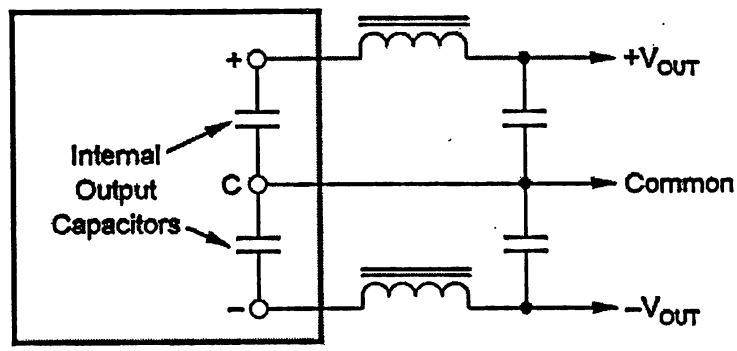

Figure2.16 Output PI filters

It is important that the inductor wire size can carry the load current, including a safety factor, and that the core does not saturate. Also notice that the dc resistance of the inductor is outside the feedback loop for regulated units and subsequently degrades that regulation. LC filters are generally used only where very accurate analog measurements are being taken, and the power supply rejection is poor at the ripple frequency. A much more common filtering technique is the output filter capacitor.

2.7.2 Output Capacitor Filtering

The basic design equations of the supply rules out any brute force approach. The parameter of major concern is the Effective Series Resistance (ESR). ESR is due to stray resistance inside the electrolytic capacitor that becomes significant at switching power supply frequencies and higher. Together with Effective Series Inductance (ESL), ESR can be modeled as the equivalent circuit shown in Figure 2.17.

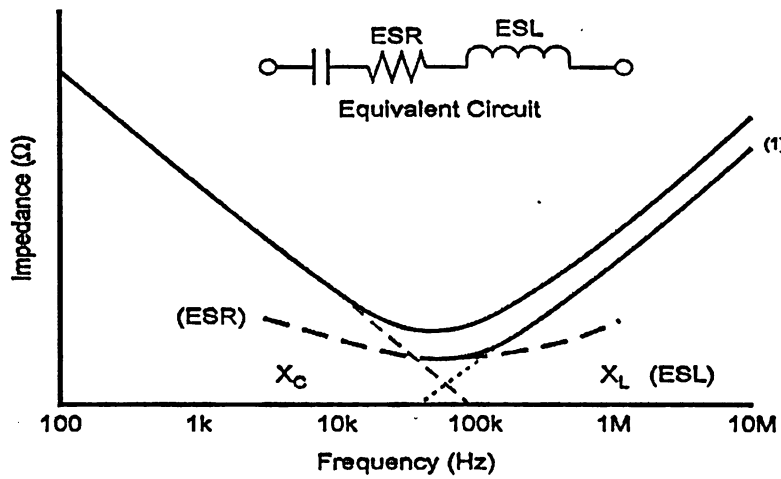

Figure 2.17 Typical log/log impedance plot for Electrolytic capacitor

ESR is also a function of temperature and actually decreases as temperature is increased. The ESR becomes, in effect, a voltage divider with the internal output resistance of the supply. Therefore, the lower the ESR, the better suited the capacitor is for filtering the output of a switching type power supply. As the load increases, the capacitors' ripple current increases, causing a larger drop across the ESR, and

consequently, a larger output ripple voltage (seen as noise). A commonly used method for estimating ESR is by means of the equation:

$$ESR = DF * 0.01/2\pi fc \qquad (2.30)$$

Where DF is given in %, f is given in hertz, and C is given in farads. Dissipation factor (DF) is a function of frequency and is useless if given at less than 1 kHz. (If given at lower frequencies, it is more indicative of equivalent parallel resistance).

It's true that good capacitors have played a big role in making switching type power supplies a technological and commercial success, but this success has inspired the capacitor makers to devise even better suited types. Because of this impetus and the versatility of the switching power supply, it is difficult to say that one type of capacitor is inherently better than another.

CHAPTER 3

Design and Analysis of SEPIC Topology

In a SEPIC (Single Ended Primary Inductance Converter) design, the output voltage can be higher or lower than the input voltage. The SEPIC is a dc/dc-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is handy when the designer uses voltages (e.g., 12 V) from an unregulated input power supply such as a low-cost wall wart.

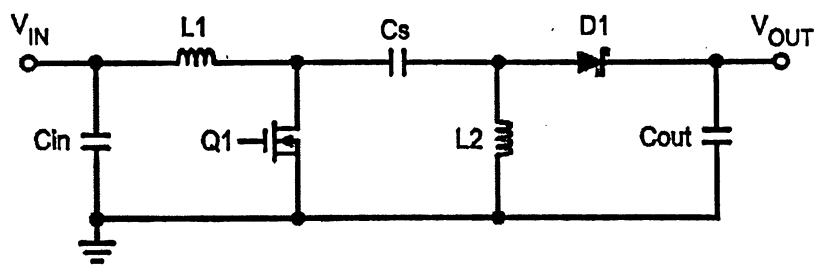

Figure 3.1 SEPIC Topology

Recently, several inductor manufacturers began selling off-the-shelf coupled inductors in a single package at a cost only slightly higher than that of the comparable single inductor. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the

inductance required for a SEPIC with two separate inductors. This article explains how to design a SEPIC converter with a coupled inductor.

3.1 Basic operation

Figure 3.1 shows a simple circuit diagram of a SEPIC converter, consisting of an input capacitor, CIN; an output capacitor, COUT; coupled inductors L1 and L2; an ac coupling capacitor, CP; a power FET, Q1; and a diode, D1. The SEPIC converter shown in Figure 1 uses two inductors, L1 and L2. The two inductors can be wound on the same core since the same voltages are applied to them throughout the switching cycle. Using a coupled inductor takes up less space on the PCB and tends to be lower cost than two separate inductors. The capacitor Cs isolates the input from the output and provides protection against a shorted load. Figure 3.2 shows the SEPIC operating in continuous conduction mode (CCM). Q1 is on and Figure 3.2 shows the SEPIC operating in continuous conduction mode (CCM). Q1 is off.

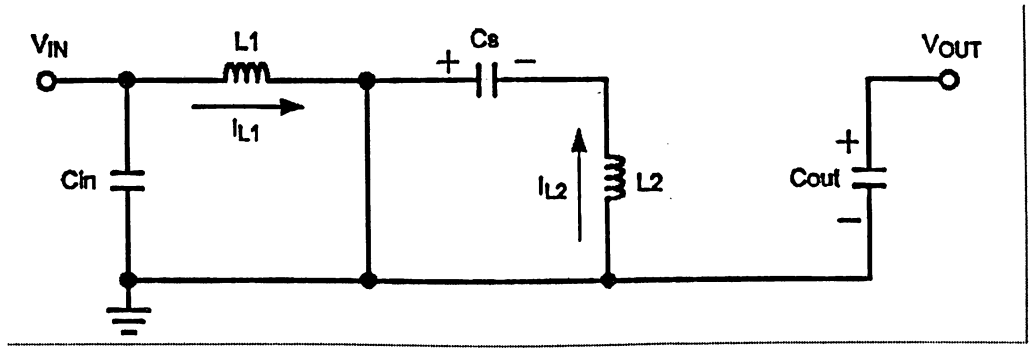

Fig3.2 SEPIC during CCM operation when Q1 is on

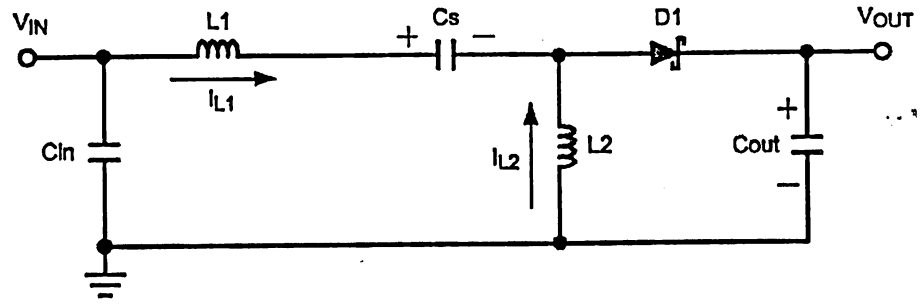

Fig3.3 SEPIC during CCM operation when Q1 is off

To understand the voltages at the various circuit nodes, it is important to analyze the circuit at dc when Q1 is off not switching. During steady-state CCM, pulse-width modulation (PWM) operation, and neglecting ripple voltage, capacitor CP is charged to the input voltage, VIN. Knowing this, we can easily determine the voltages as shown in Figure 3.4.

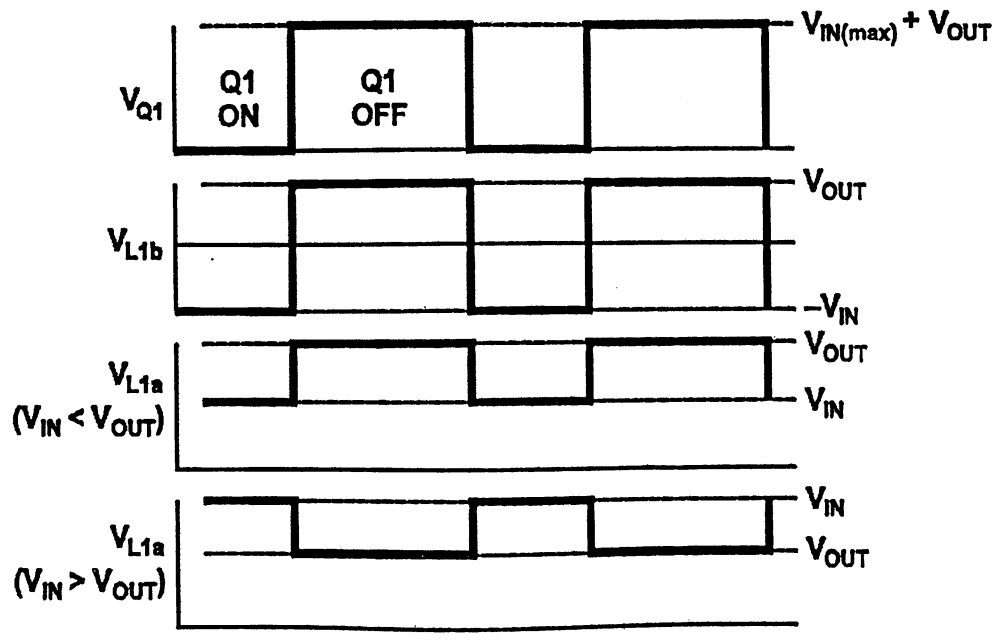

Fig3.4 SEPIC component voltage during CCM

When Q1 is off, the voltage across L1b must be VOUT. Since CIN is charged to VIN, the voltage across Q1 when Q1 is off is VIN + VOUT, so the voltage across L1a is VOUT. When Q1 is on, capacitor CP, charged to VIN, is connected in parallel with L1b, so the voltage across L1b is –VIN.

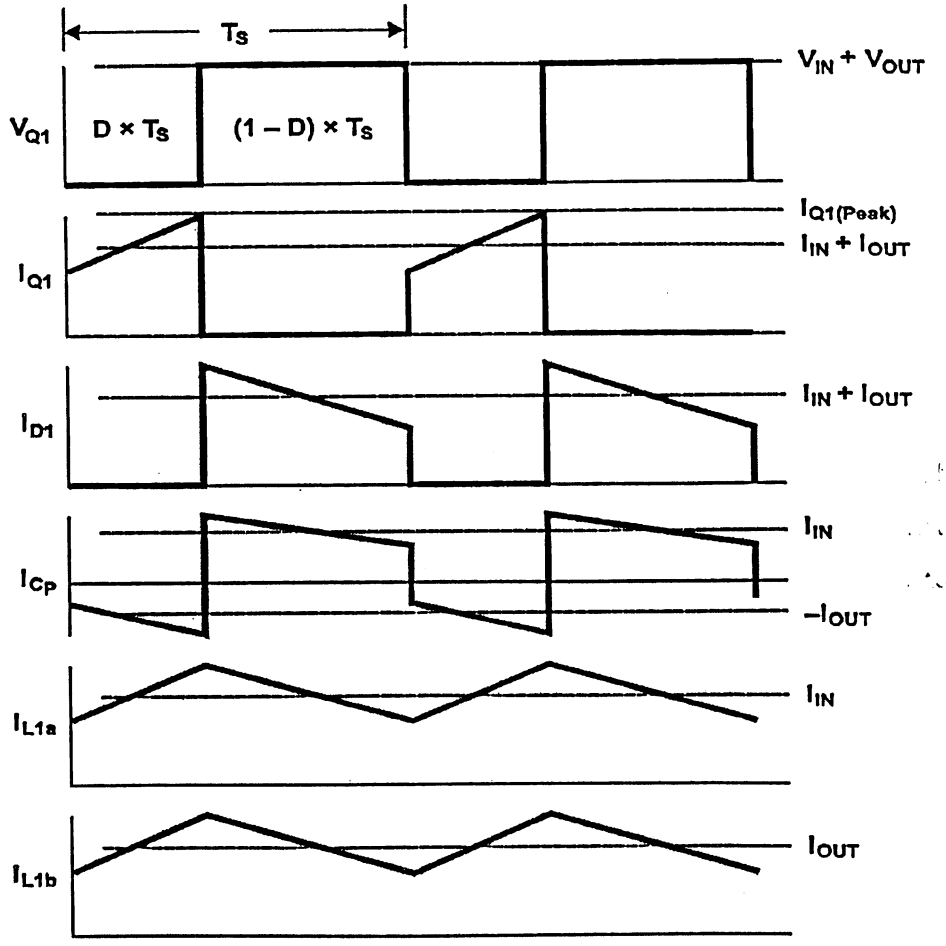

Fig3.5 SEPIC component currents during CCM

The currents flowing through various circuit components are shown in Figure 3.5. When Q1 is on, energy is being stored in L1a from the input and in L1b from CP. When Q1 turns off, L1a's current continues to flow through CP and D1,

and into C_{OUT} and the load. Both C_{OUT} and C_P get recharged so that they can provide the load current and charge L_{1b}, respectively, when Q_1 turns back on.

3.2 Component Selection

3.2.1Duty Cycle Consideration

For a SEPIC converter operating in a continuous conduction mode (CCM), the duty cycle is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D} \tag{3.1}$$

V_D is the forward voltage drop of the diode D1. The maximum duty cycle is:

$$D = \frac{V_{OUT} + V_D}{V_{IN(min)} + V_{OUT} + V_D} \tag{3.2}$$

3.2.2 Inductor Selection

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_l = I_{IN} \cdot 40\% = I_{out} \cdot \frac{V_{out}}{V_{in(min)}} \cdot 40\% \quad (3.3)$$

The inductor value is calculated by:

$$L_1 = L_2 = L = \frac{V_{in(min)}}{\Delta I_L \cdot f_{sw}} \cdot D_{max} \quad (3.4)$$

f_{sw} is the switching frequency and D_{max} is the duty cycle at the minimum Vin. The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1(peak)} = I_{out} \cdot \frac{V_{OUT} + V_D}{V_{IN(min)}} \cdot \left(1 + \frac{40\%}{2}\right) \quad (3.5)$$

$$I_{L2(peak)} = I_{out} \cdot \left(1 + \frac{40\%}{2}\right) \quad (3.6)$$

If L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN(min)}}{2 \cdot \Delta I_L \cdot f_{sw}} \cdot D_{max} \quad (3.7)$$

3.2.3 Power MOSFET Selection

The parameters governing the selection of the MOSFET are the minimum threshold voltage Vth(min), the on-resistance RDS (ON), gate-drain charge QGD, and the maximum drain to source voltage, VDS(max). Logic level or sublogic-level

threshold MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to Vin + Vout. The peak switch current is given by:

$$I_{Q1(peak)} = I_{L1(peak)} + I_{L@(peak)} \quad (3.8)$$

The RMS current through the switch is given by:

$$I_{Q1(rms)} = I_{out} \sqrt{\frac{(V_{OUT} + V_{IN(min)} + V_D) \cdot (V_{OUT} + V_D)}{V_{IN(max)}^2}} \quad (3.9)$$

The MOSFET power dissipation PQ1 is approximately:

$$P_{Q1} = I_{Q1(rms)}^2 \cdot R_{DS(on)} \cdot D_{max} + (V_{IN(min)} + V_{OUT}) \cdot I_{Q1(peak)} \cdot \frac{Q_{GD} \cdot f_{sw}}{I_G}$$

PQ1, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. IG is the gate drive current. The RDS(ON) value should be selected at maximum operating junction temperature and is typically given in the MOSFET datasheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

3.2.4 Output Diode Selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current IQ1 (peak). The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1} = V_{IN(\max)} + V_{OUT(\max)} \quad (3.10)$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

3.2.5 SEPIC Coupling Capacitor Selection

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by:

$$I_{Cs(rms)} = I_{out} \cdot \sqrt{\frac{V_{OUT} + V_D}{V_{IN(min)}}} \quad (3.11)$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic

capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating. The peak-to-peak ripple voltage on Cs (assuming no ESR):

$$\Delta V_{cs} = \frac{I_{out} \cdot D_{max}}{Cs \cdot f_{dw}} \quad (3.12)$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage.

3.2.6 Output Capacitor Selection

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor must be capable of handling the maximum RMS current. The RMS current in the output capacitor is:

$$I_{Cout(rms)} = I_{out} \cdot \sqrt{\frac{V_{OUT} + V_D}{V_{IN(min)}}} \quad (3.13)$$

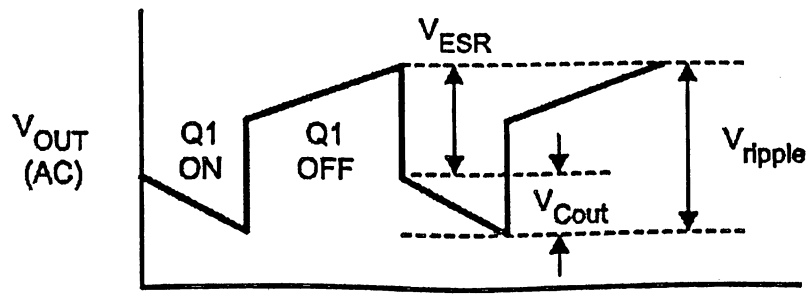

Figure 3.6 Output Ripple Voltage

The ESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. As shown in Figure 4, we assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence,

$$ESR \leq \frac{V_{ripple} \cdot 0.5}{I_{L1(peak)} + I_{L2(peak)}} \tag{3.14}$$

$$C_{out} \geq \frac{I_{out} \cdot D}{V_{ripple} \cdot 0.5 \cdot F_{sw}} \tag{3.15}$$

The output cap must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{Cin(rms)} = \frac{\Delta I_L}{\sqrt{12}} \tag{3.16}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 μF or higher value, good quality capacitor would prevent impedance interactions with the input supply.

3.3 SEPIC Converter Design parameter

Table.3.1

Input Voltage (V_I)	100 volt
Output Voltage (V)	60 volts
Switching Frequency (f_s)	50 kHz
Switching Time (T_s)	20 μs
Power (P)	100 W
Resistance (R_{nom})	100 Ω
Transformer turn ratio (N)	1

3.3.1 Duty cycle calculation

We assume that the V_D is 0.5V, then D_{max} can be given as

$$D_{max} = \frac{60 + 0.5}{100 + 60 + 0.5} = 0.38 \quad (3.17)$$

3.3.2 Inductor calculation

The input inductor L1 ripple current is:

$$I_{out} = \frac{P}{V_{out}} = \frac{100}{60} = 1.67 \quad (3.18)$$

$$\Delta I_L = 1.67 * \frac{60}{100} * 40\% = 0.40 \quad (3.19)$$

and the inductance for L1 and L2 is:

$$L1 = L2 = L = \frac{100}{0.40 * 50 * 10^3} * 0.38 = 190\mu H \quad (3.20)$$

3.3.3 Output diode calculation

The rated reverse voltage of the diode must be higher than VIN+VOUT and the average diode current is equal to the output current at full load.

3.3.4 SEPIC coupling capacitor selection

The RMS current of the Cs is:

$$I_{Cs(rms)} = 1.67 * \sqrt[2]{\frac{60 + 0.5}{100}} = 0.91\,A \quad (3.21)$$

and the ripple voltage is:

$$\Delta V_{cs} = \frac{1.67 * 0.38}{0.20 * 10^{-6} * 50 * 10^{3}} = 63.46 \text{ volt} \quad (3.22)$$

3.3.5 Output capacitor selection

The RMS current of the output capacitor is:

$$I_{Cout(rms)} = I_{CS(rms)} = 0.91 \text{ A} \quad (3.23)$$

Assuming the peak-to-peak ripple is 2% of the 100 V output voltage, the ESR of the output capacitor is:

$$ESR \leq \frac{V_{ripple} \cdot 0.5}{I_{L1(peak)} + I_{L2(peak)}}$$

and the capacitance is:

$$C_{out} \geq \frac{1.67 * 0.38}{100 * 0.02 * 0.5 * 50 * 10^{3}} = 12 * 10^{-6} = 12\mu F \quad (3.24)$$

12μF ceramic capacitor is used. For cost-sensitive applications, an electrolytic capacitor and a ceramic capacitor can be used together. Noise sensitive applications can include a second stage filter.

3.4 Hysteresis Current Control Strategy

Since the PWM control strategy is used in the area of the rectifier, particularly with the development of DSP control devices and the IGBT power devices, hysteresis current control rectifier do attract with its advantages such as easy to implement, fast dynamic response and low sensitive to the system parameters and the load [1].

However, the traditional hysteresis current control strategy not only led to too high switching frequency of the problem, but also in actual system the voltage outer-loop PI parameters tuning is a major difficulty. Therefore, this paper from the optimization of the reference current of hysteresis PWM rectifier and to lower the traditional current hysteresis PWM rectifiers of switching frequency point of view, not only proposes a way to limit the maximum switching frequency and reduce switching frequency of changes, but also introduces load current feed-forward control to achieve large-scale increase the three-phase PWM Voltage Rectifier of the outer-loop PI parameters range, making it easier to set more simple and effective.

Hysteresis current control principle is shown in fig.3.7. Its core idea is that the real-time actual current signal i be compared to the reference current signal i^* in the process of operation: if i is greater than the upper limit $i^* + h$, turn on the bridge on the arm to decreased i; if i is less than lower limit $i^* - h$, turn off the bridge under to increase i, where h is defined as the hysteresis width. Through the control method the actual current i can be controlled within a fixed range.

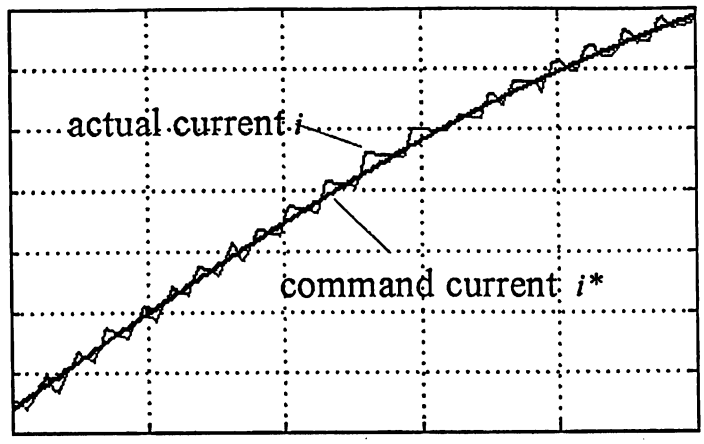

Figure 3.7 Reference current and the actual current

In the process of hysteresis comparison, the real-time actual current value i is tracking of the reference current signal i * through fluctuations. As i * has the same phase with the input three-phase voltage, with the process of following the tracks of i * , the actual current value i achieves to has the same phase as the real input voltage phase, thereby ,achieved the control requirement of high power factor, as shown in fig.3.7.

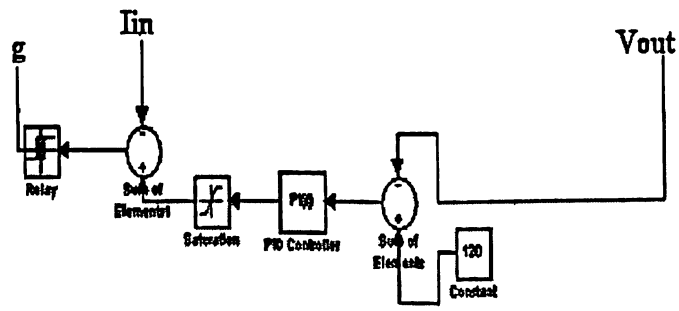

Figure 3.8 Control circuit for the proposed converter.

3.5 Conclusions of the Chapter

In this chapter we have analyzed about the designing and analysis of the SEPIC topology based dc-dc converter. Here we studied that how a SEPIC converter operates. Duty cycle and selection of active and passive components for SEPIC converter are also explained. Further we derived the model equation for SEPIC system. Critical conduction parameters have been also discussed. We have deliberated about the designing of inductors L_1, L_2 and intermediate capacitor C_1. Finally in this chapter we explained about the hysteresis control strategy.

CHAPTER 4

Simulated Circuit View

- **Simulation of Buck-Boost System**

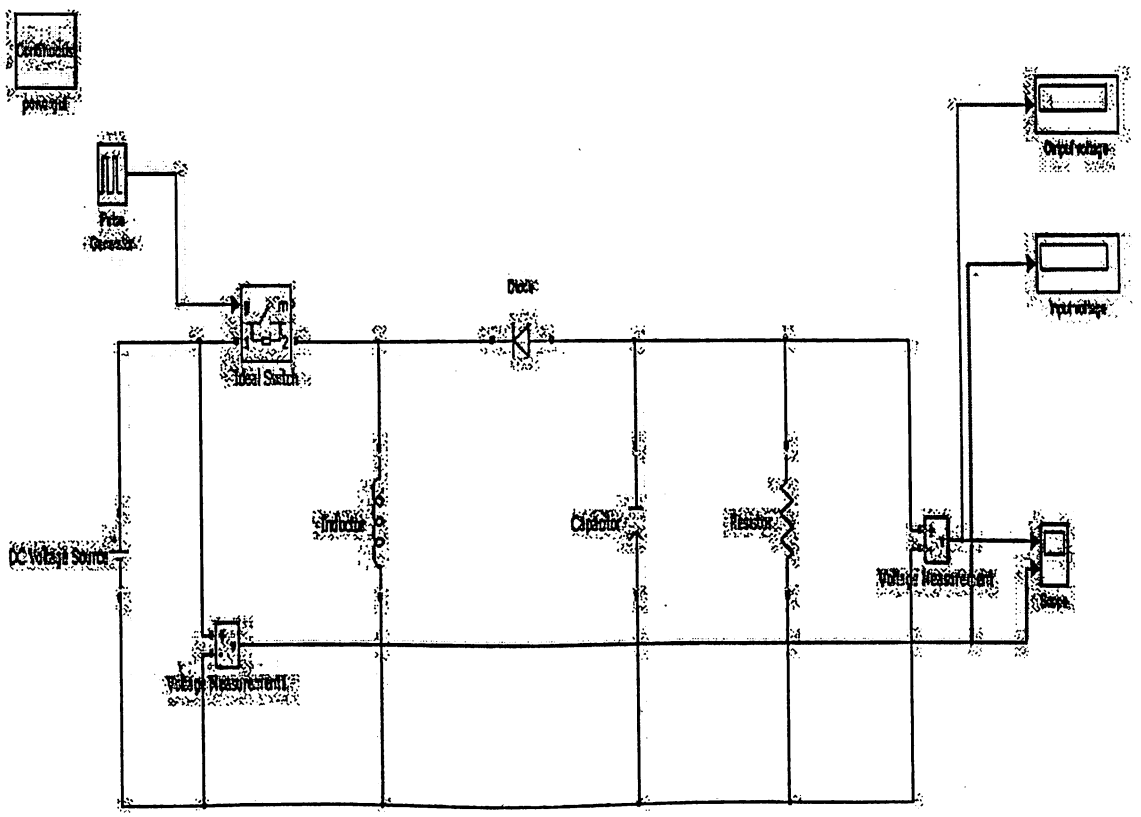

Fig. 4.1 Buck-Boost Circuit

➢ Simulation of Cuk System

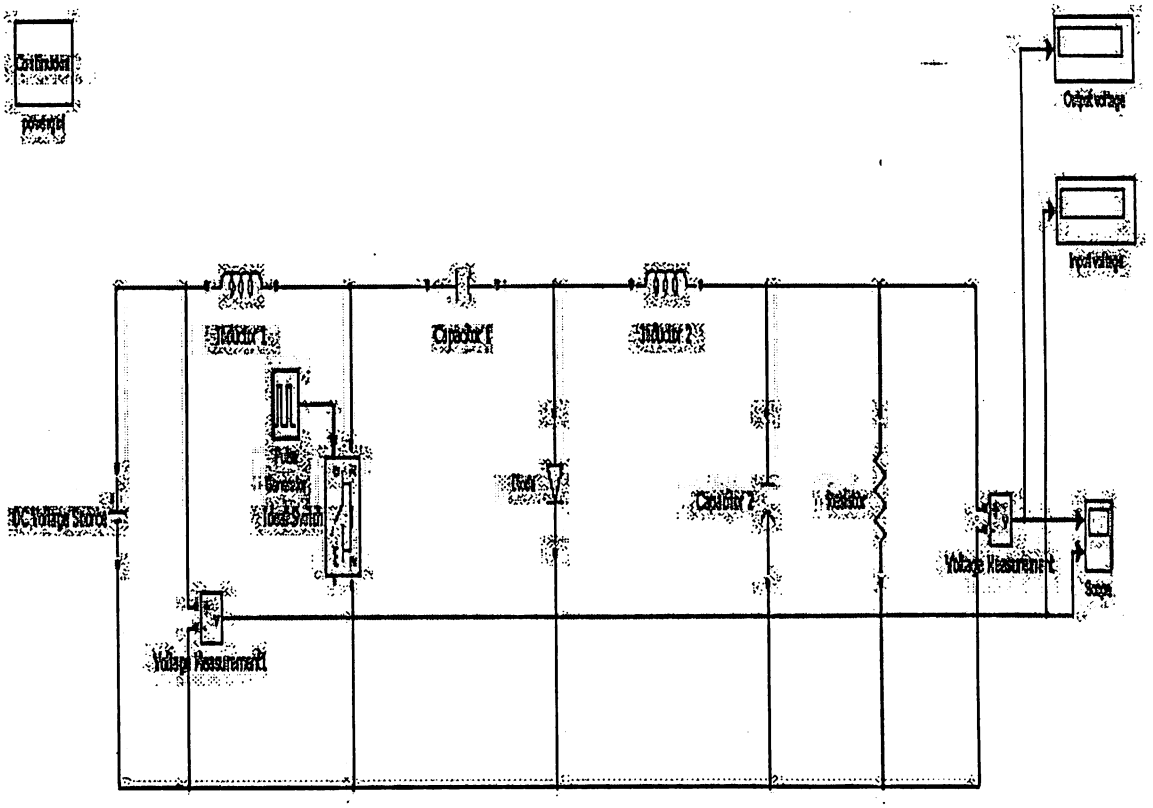

Fig. 4.2 Cuk Circuit

➢ Simulation of Chopper System

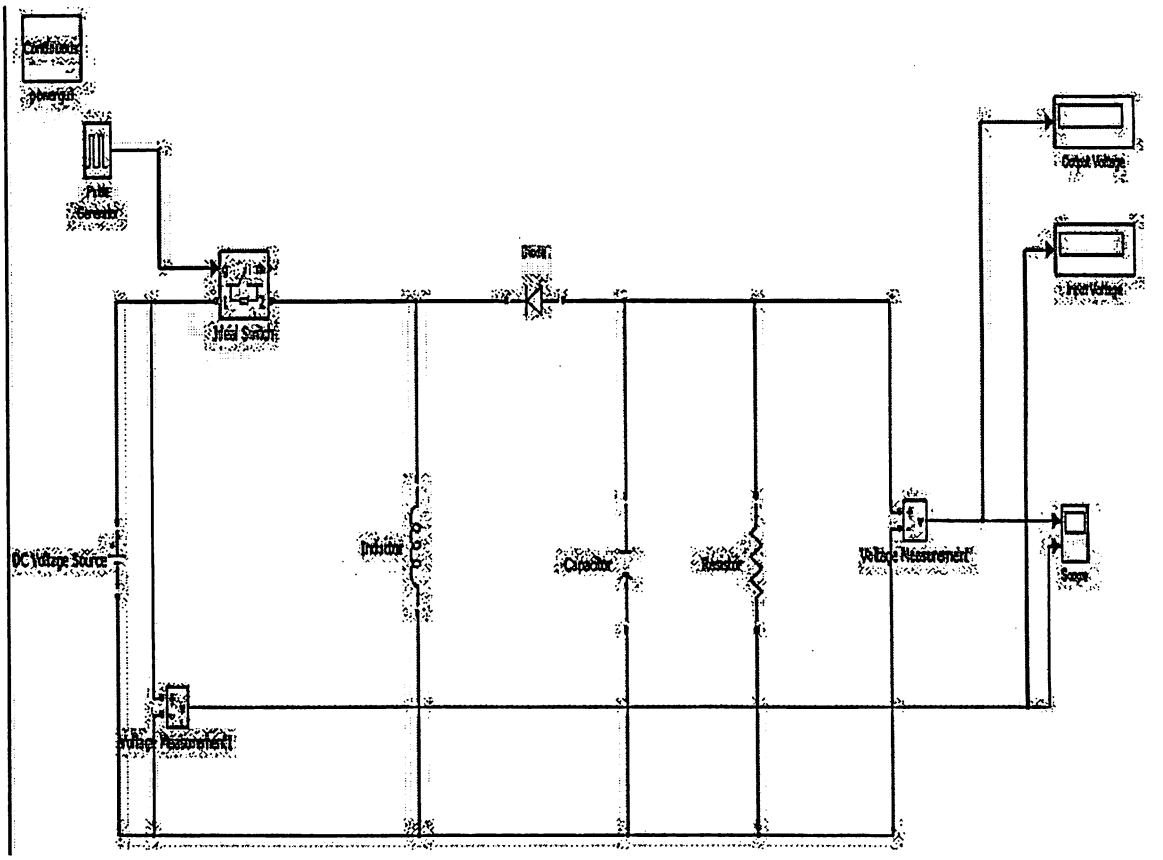

Fig. 4.3 Chopper Circuit

➢ Simulation of SEPIC System

Open loop SEPIC system

The simulation circuit of SEPIC system is shown in fig as given below. This circuit contains dc voltage source V, a mutual inductor MU, a switch Sw, a diode D, two capacitors C1 and Co and a load resistance Ro. The values of circuit parameters are taken according to the designed values. The gate pulse is generated by a pulse generator for the switching of switch Sw.

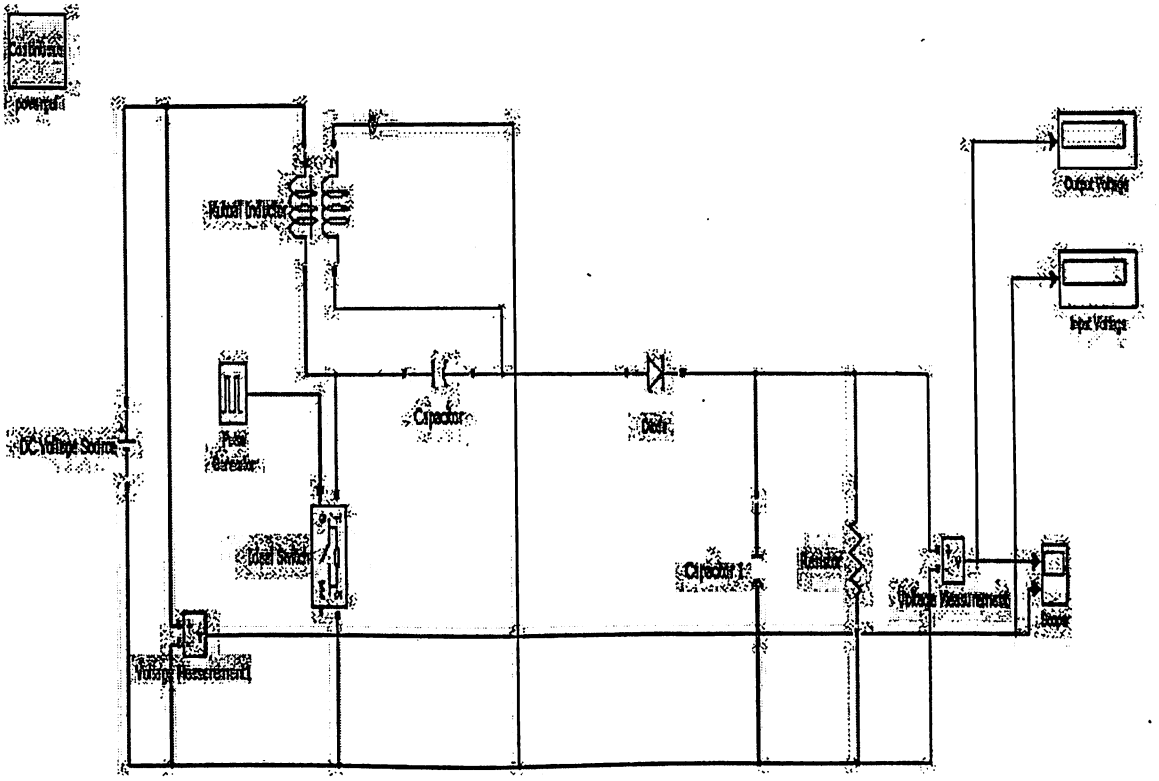

Fig. 4.4 Open loop simulation circuit of SEPIC system

Closed Loop Simulation Circuit of SEPIC

The closed loop simulation circuit of proposed SEPIC system is shown in Fig.4.5. In the closed loop circuit all the circuit parameters are the same as for the open loop circuit the only difference is that we have a simple hysteresis current control scheme for the generation of the gate pulse for the switch Sw instead of a pulse generator as in open loop simulation circuit. In the hysteresis current control scheme the output voltage is being compared with the desired voltage in sum block then the output of this sum block is processed by a PID block and saturation block subsequently, then the output of saturation block is compared with the input current in an another sum block which output is fed to a relay. Finally the output of the relay which is also known as control signal for the switch Sw is given to the gate terminal of switch Sw. This control signal works as a gate pulse for the switch to turn ON and turn OFF to maintain the desired output at load side as a gate pulse for switching action.

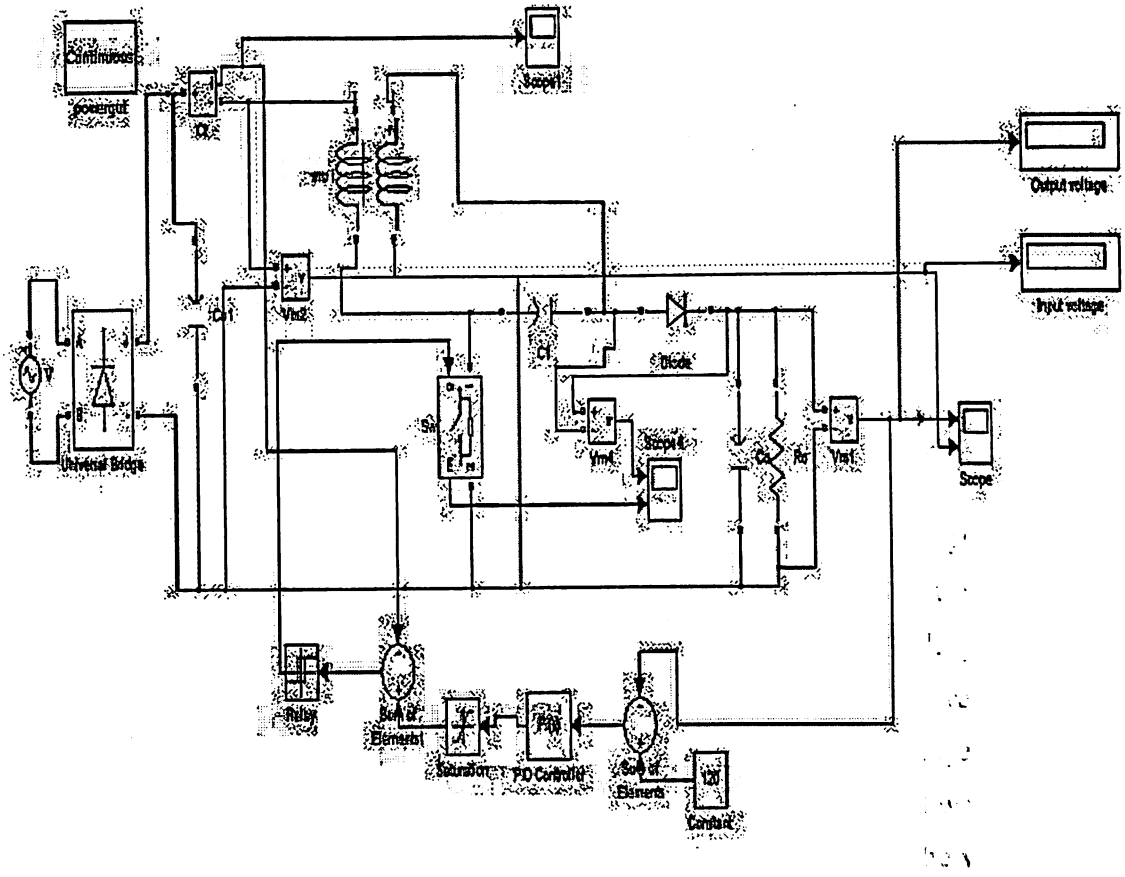

Fig.4.5 Close loop simulation circuit of SEPIC system

Performance Analysis

This section presents the output waveforms evaluation of the proposed SEPIC converter. Fig.4.6 illustrates the measured waveform of output voltage. Hysteresis current control scheme is used for current controlling. Input voltage V_{in} is 100 volt and reference voltage is 60 volt is taken. In the control process reference current is compared with actual current. The wave form for output voltage V_{out} is shown in the Fig.4.6. In the proposed converter Mutual inductance is used which has a primary side L_1 and secondary side L_2. It has ripple free output. Here the value of

L_1 is 1.83 mH and L_2 is 128μH. Fig.4.7 and Fig.4.8 shows the waveform of inductor voltage V_{L1} and V_{L2} in steady state respectively.Wave forms shown in Fig.4.9 illustrate the voltage V_d across the diode D in steady state. Fig.4.10 and Fig.4.11 shows the capacitor voltage V_{c1} in transient and steady state. And Fig.4.12 indicate that how the inductor current I_{L1} varies in hysteresis control scheme. This measured current is being compared with the reference current to generate appropriate gate pulse for switch S_w. And thus the output voltage is being fixed at desired value. Fig.4.6 shows the waveform for the output voltage.

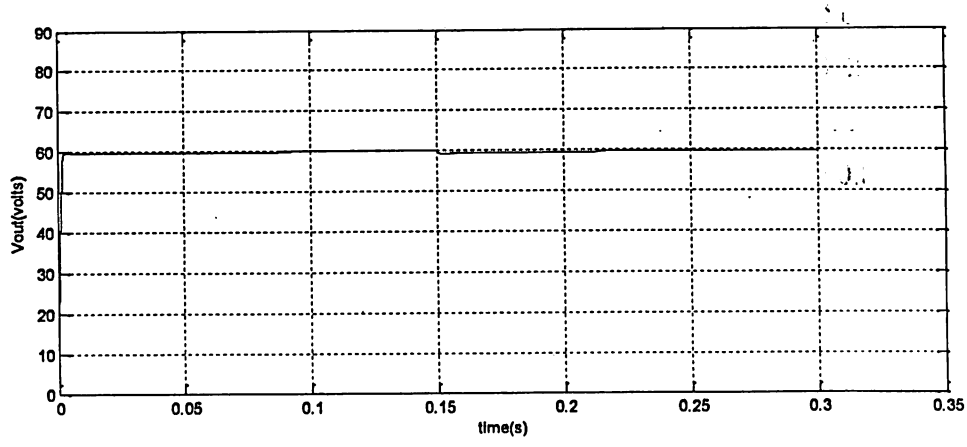

Fig.4.6: Output voltage V_{out}.

As in Fig.4.6 we can observe that the output voltage V_{out} across the load increases sharply and attains the voltage level of 60 volts in 0.001 sec. So the rise time (t_r) will be 0.001 sec for this wave form. And it settles after 0.002 sec. to maintain the constant voltage. The settling time is 0.002 for this waveform. The maximum value is achieved within 0.003 sec. So the peak time (t_p) will be 0.003 sec.

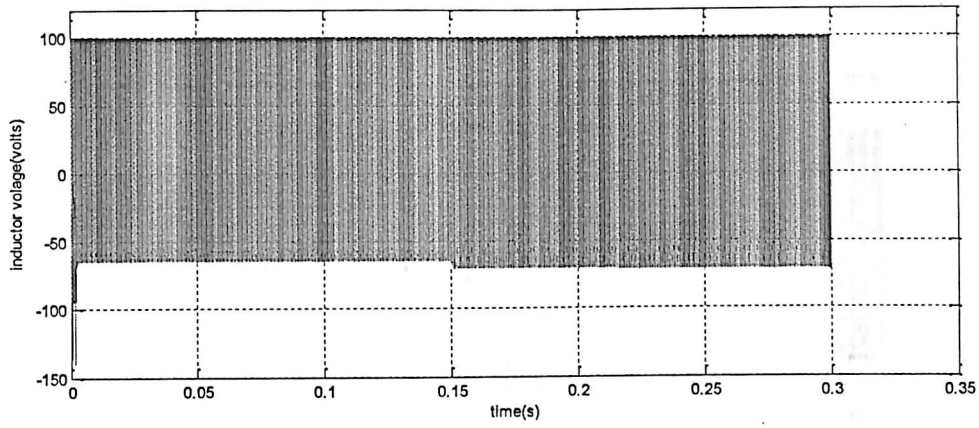

Fig.4.7: Inductor Voltage [V_{L1}] in steady state.

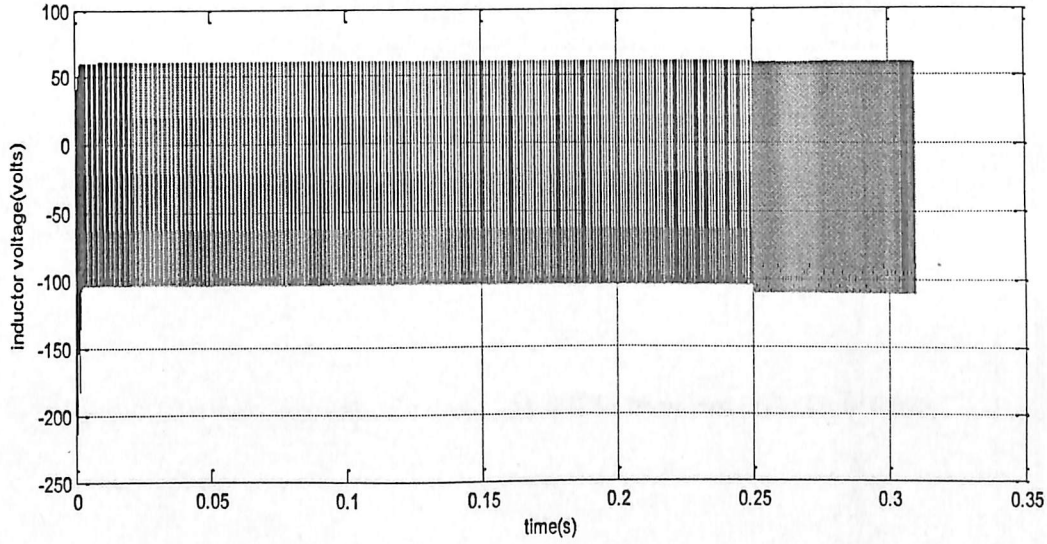

Fig.4.8: Inductor Voltage [V_{L2}] in steady state.

Fig.4.7 shows the primary Inductor voltage [V_{L1}] across the primary inductor and secondary Inductor voltage [V_{L2}] is shown in Fig.4.8. From both the figure we can see that the inductors are coupled to each other as both the signals are opposite in phase.

The voltage across the diode in steady state is shown in Fig.4.9.

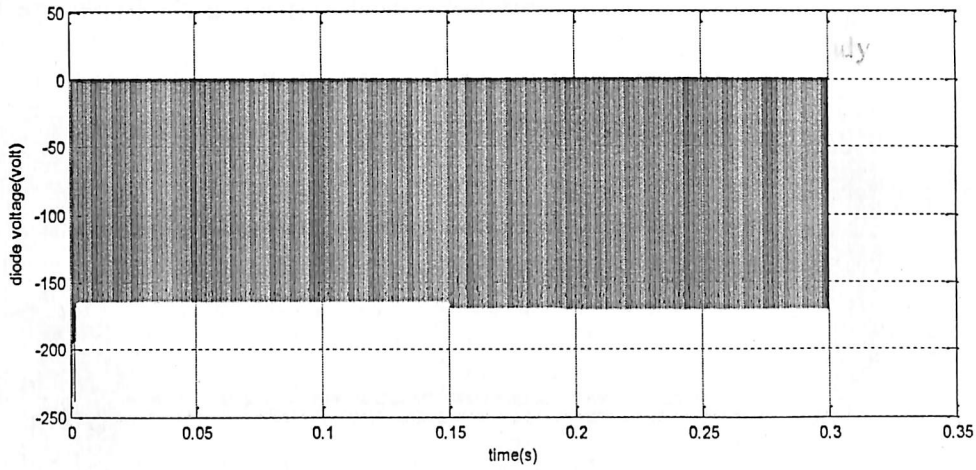

Fig.4.9: Diode Voltage [V_d] in steady state.

Fig.4.10 and Fig.4.11 shows the capacitor voltage V_{c1} in transient and steady state.

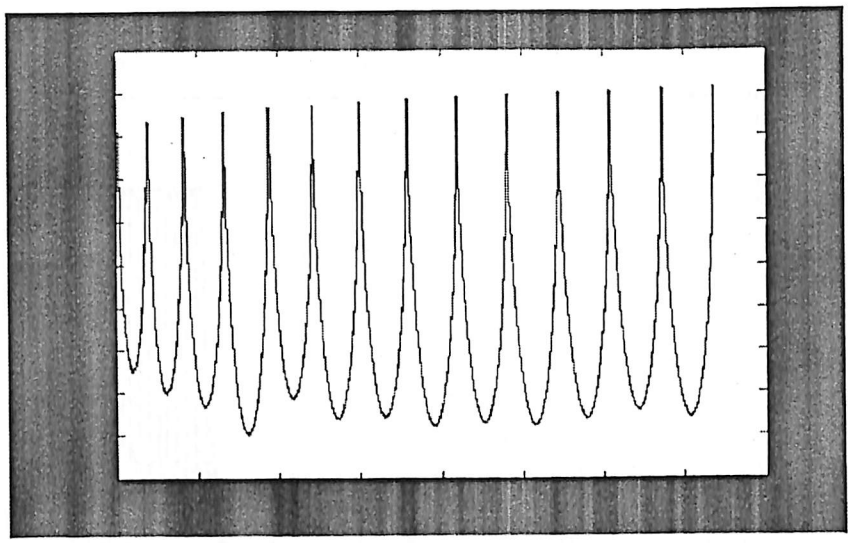

Fig.4.10: Capacitor Voltage [V_{c1}] in transient state.

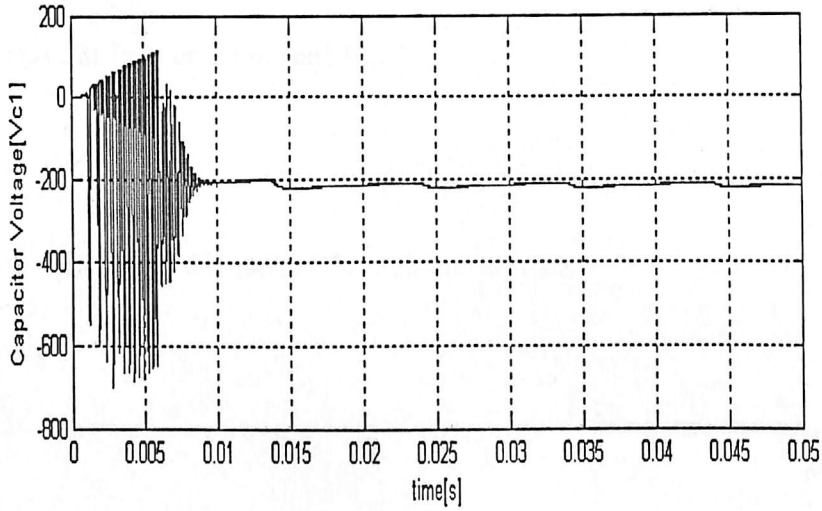

Fig.4.11: Capacitor Voltage [V_{c1}] in steady state.

Fig.4.12 shows that how the inductor current I_{L1} varies with the operation of closed loop hysteresis current control system.

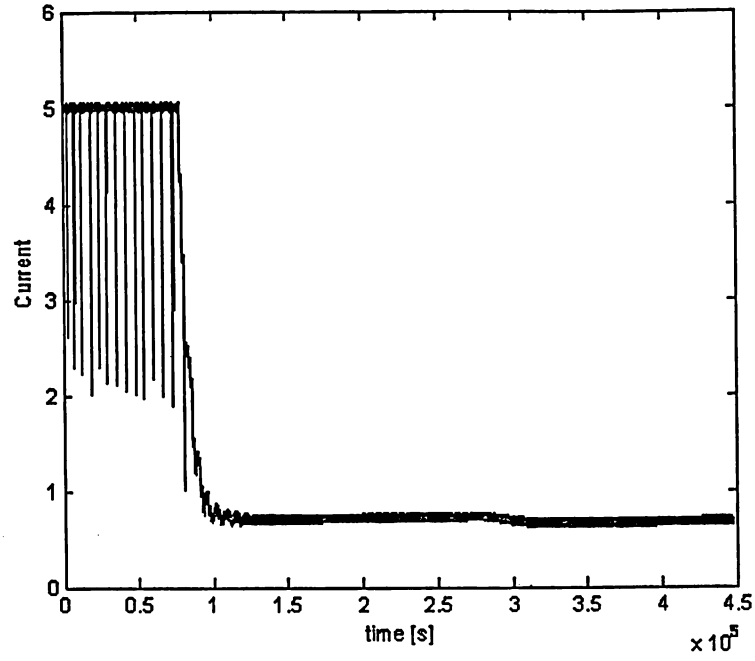

Fig.4.12: Inductor current I_{L1}.

Fig.4.13 shows the current through inductor L_2.

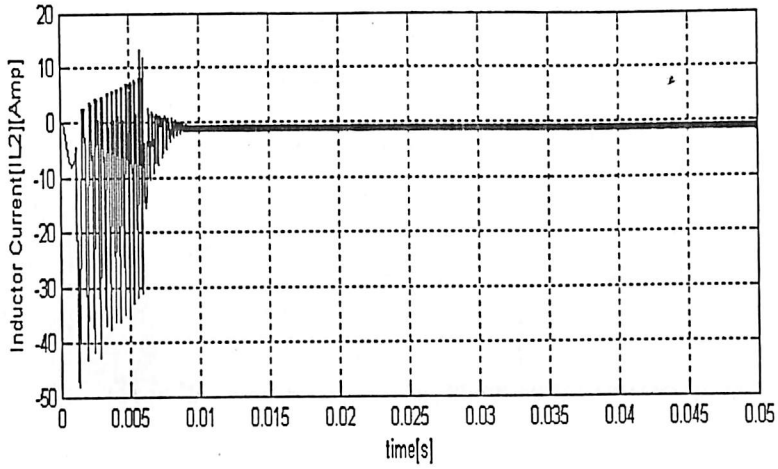

Fig.4.13: Inductor current I_{L2}.

Fig.4.14 shows the current through intermediate capacitor C_1.

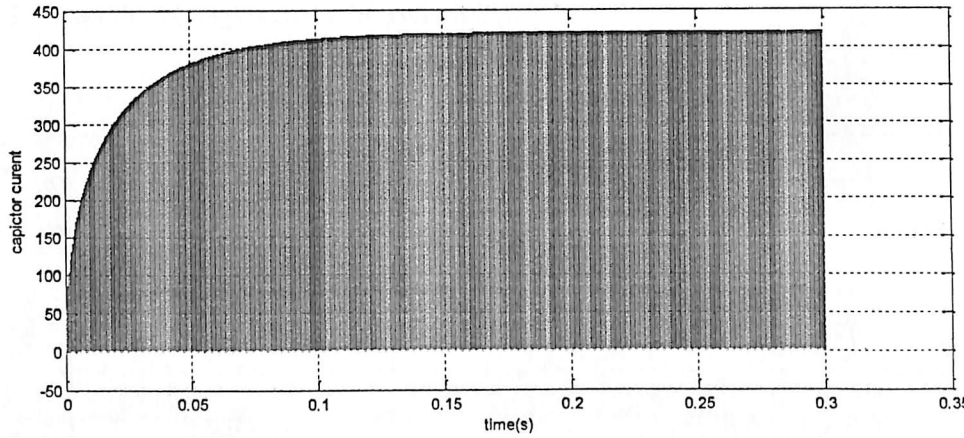

Fig.4.14: Capacitor current I_{C1}.

Fig.4.15 shows the current through diode D.

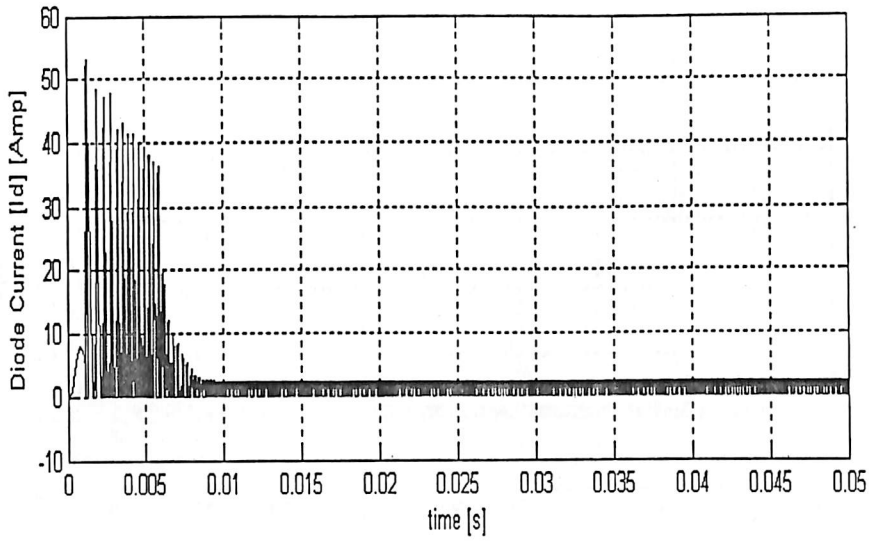

Fig.4.15: Diode current I_d.

Fig.4.16 shows the voltage across the switch Sw.

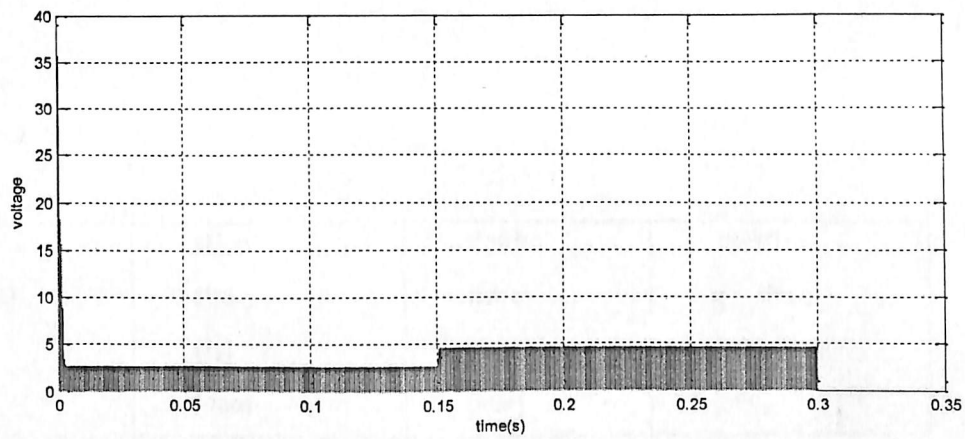

Fig.4.16: Voltage across switch Sw.

Fig.4.17 shows the current through switch Sw.

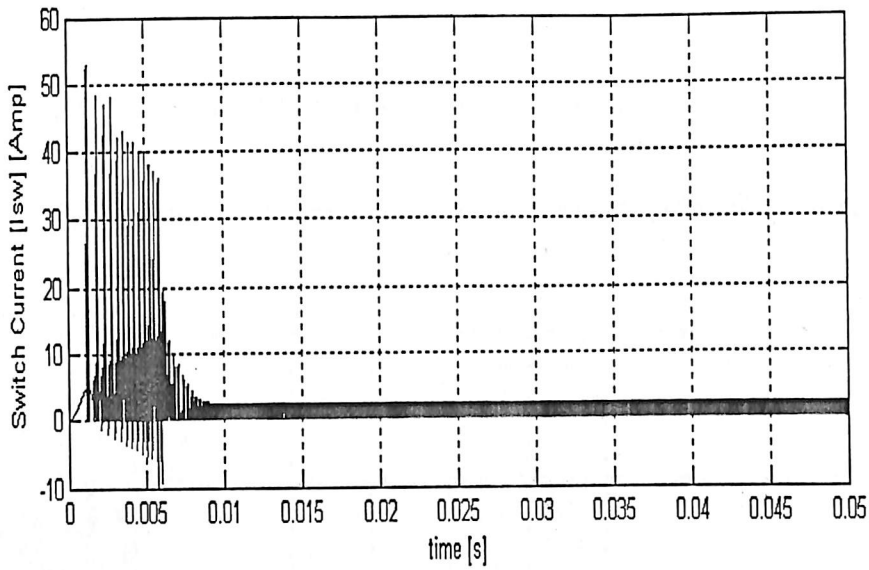

Fig.4.17: Switch current Isw.

Rise time (t_r) , Peak time (t_p) , Settling time (t_s) for Different Output Voltages

Table.4.1

V_{out} (volts)	Rise time (t_r) [sec]	Peak time (t_p) [sec]	Settling time (t_s) [sec]
60	0.007	0.009	0.010
80	0.012	0.013	0.014
120	0.025	0.026	0.027
110	0.022	0.024	0.025
70	0.009	0.011	0.012

Output Voltage at Different Reference Voltages

A: Fig.4.18 shows the Output voltage when the reference voltage is set to 80 volts.

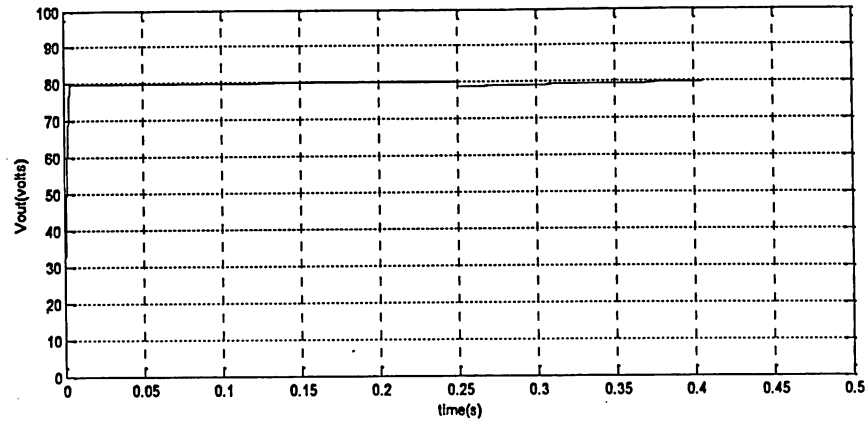

Fig.4.18: Output voltage when V_{ref} is 80 volts.

B: Fig.4.19 shows the Output voltage when the reference voltage is set to 120 volts.

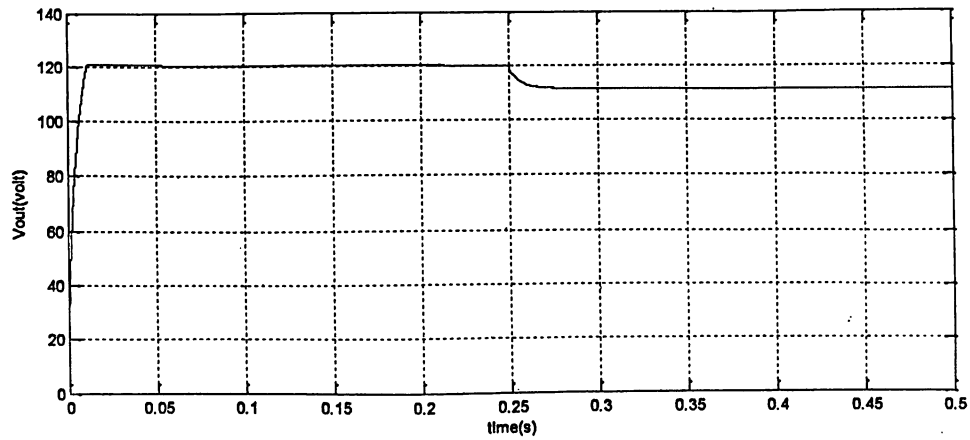

Fig.4.19: Output voltage when V_{ref} is 120 volts.

C: Fig.4.20 shows the Output voltage when the reference voltage is set to 110 volts.

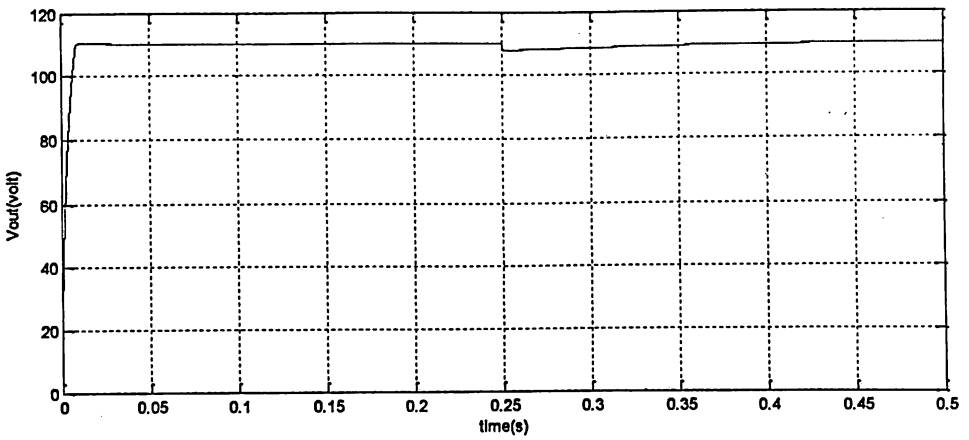

Fig4.20: Output voltage when V_{ref} is 110 volts.

D: Fig.4.21 shows the Output voltage when the reference voltage is set to 70 volts.

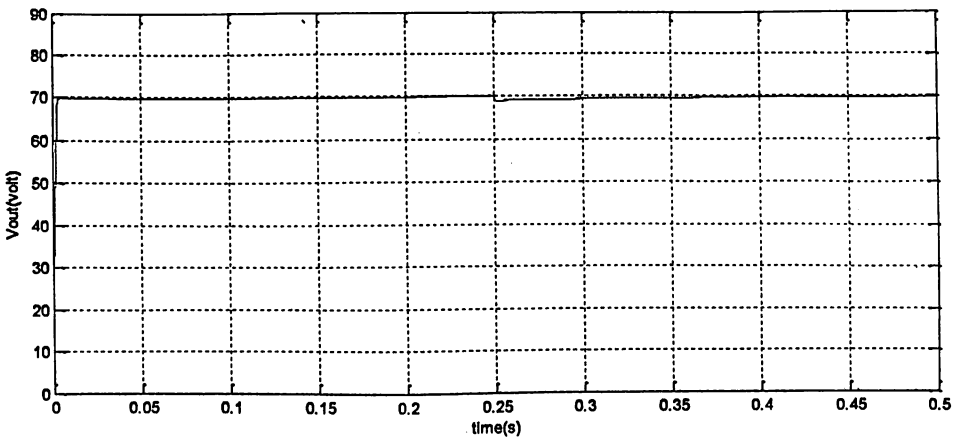

Fig.4.21: Output voltage when V_{ref} is 70 volts.

CHAPTER 5

RESULT

S.No.	Name of Converter	Formula	Output at D= 40%	Output at D= 50%	Output at D= 60%	Nature of Output Voltage
1.	Buck Boost	V_o/V_i=-D/(1-D)	V_o=-79.3V T_r=0.0955s	V_o=-119.4V T_r=0.0955s	V_o=-179.2 T_r=0.09555s	Inverted Polarity
2.	Chopper	V_o/V_i=-D/(1-D)	V_o=-79.5V T_r=0.092s	V_o=-119.2V T_r=0.194s	V_o=-179.2V T_r=0.196s	Inverted Polarity
3.	Cuk	V_o/V_i=-D/(1-D)	V_o=-78.9V T_r=0.0996s	V_o=-118.7V T_r=0.0174s	V_o=-178.1V T_r=0.0495s	Inverted Polarity
4.	SEPIC	V_o/V_i=-D/(1-D)	V_o=79.29V T_r=0.092s	V_o=119.4V T_r=0.0865s	V_o=179.6V T_r=0.0865s	Non-Inverted Polarity
5.	SEPIC (closed loop)	Depends on V_{ref}	V_o=79.81V T_r=0.004s	V_o=119.5V T_r=0.004s	V_o=179.1V T_r=0.0065s	Non-Inverted Polarity

CHAPTER 6

Conclusions and Future Scope

6.1 Conclusions

By introducing SEPIC converter in the solar power system, the power quality will improved. In this study we understood how SEPIC Topology is useful in the solar power system. The power is transmitted from one place to another with the help of conductors, in this power transmission some losses occurs in the conductor. With SEPIC converter the voltage level is increased which can reduce the losses while transmitting the power. The reduction of losses will improve the quality of power and effectiveness of power.

The DC Solar power is stored in batteries, for storing the DC power we need converters. To supply a desired amount of voltage which can easily be stored in batteries. With the help of SEPIC we can step up the DC voltage according to the Desired need of Battery The modified SEPIC circuit provides lower conduction losses with reduced components simultaneously. In conventional PFC converters

The modified SEPIC circuit provides lower conduction losses with reduced components simultaneously. In conventional PFC converters (CCM boost converter) a voltage loop and a current loop are needed for power factor correction. Boost converter has also several disadvantages as follows:

1: Input-output isolation cannot be easily implemented.

2: The output voltage is always higher than the peak input voltage.

3: Overload and start-up over current cannot be controlled because there is no series switch between input and outpu.

The simulation on MATLAB has been verified the practicability of the SEPIC converter. SEPIC converter with low input current distortion and low conduction losses has been presented and analyzed. The proposed converter is derived from the conventional SEPIC and Cuk converters. The SEPIC circuit has lower conduction loss and switching loss, the proposed topology can further improve the conversion efficiency. The input current obviously follows the input voltage; therefore theoretically power factor is one. The ripple present in the input current is restricted by design, selecting a satisfactory value for the input inductor (L_1). A proper selection of the intermediate capacitor C_1 is essential in obtaining a high quality input current. To keep up same efficiency, this advanced SEPIC circuit could function with higher switching frequency. As a result, auxiliary reduction in the dimension of inductor could be achieved. Besides improving circuit topology and performance, a further reduction in SEPIC converter size has been realized by integrating the two inductors into a single magnetic core. The modified SEPIC converter has been simulated on a 100-W prototype at 120-V output voltage to show high performance in terms of high power factor and efficiency.

6.2 Future Scope of the work

This dissertation work has provided the basis for realizing the improvements of SEPIC based dc-dc converter with integrated electronics. The reduction in SEPIC converter size has been realized by integrating the two inductors into a single magnetic core. Future research directions will focus on higher level integration and reducing the cost of power transmission of power from one place to another. As explainer in this research, day by day the size of converter is reduced which may acquire less space to install. With the help of this size reduction, the converter take very less space for installation.

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