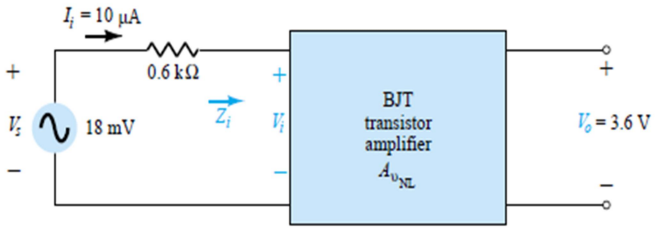
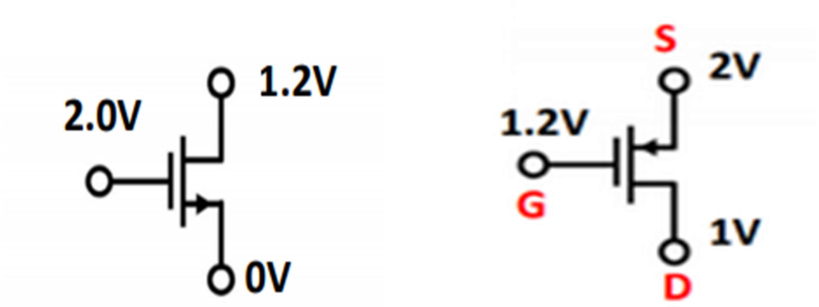
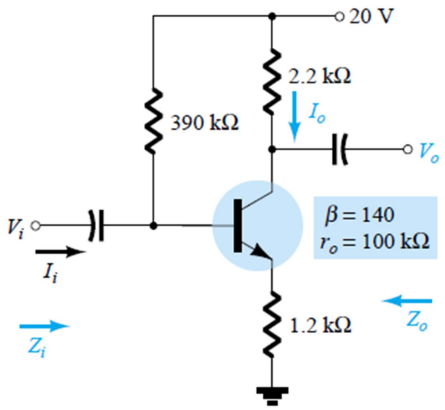
Name: Enrolment No:	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, Dec 2021

Programme Name: B.Tech ECE **Semester: III**
Course Name: Analog Electronics I. **Time: 03 hrs**
Course Code: ECEG 2011 **Max. Marks: 100**
Nos. of page(s): 4

S. No.	**SECTION A : (4X5 = 20 M)** **Attempt all the questions**	**Marks**	**COs**
Q 1	For a given the BJT configuration as shown in Fig 1 below, determine: (a) V_i. (b) Z_i. (c) Av_{NL} (d) A_{vs}.  Fig1	4	CO1
Q 2	Determine the oprating region for the given MOSFET configurations as shownin fig 2?  Fig. 2	4	CO2

Q 3	Sketch the equivalent hybrid model for CE npn BJT and mention all the hybrid model parameters.	**4**	**CO1**
Q4	Explain the pinch off condition in JFETs and its impact over the drain current. Sketch the N channel JFET with proper regions?	**4**	**CO2**
Q5	Mention the impact of cascade network of amplifiers on the overall gain and the bandwidth of the amplifier. Explain by considering the frequency response?	**4**	**CO4**
SECTION B : (4X10 = 40M) **Attempt All the questions**			
Q 6	Sketch the curve of $I_D = 0.5*10^{-3}(V_{GS})^2$ and $I_D = 0.5*10^{-3}(V_{GS} - 4)^2$ for V_{GS} from 0 to 10 V. Does $V_T = 4$ V have a significant impact on the level of I_D for this region?	**10**	**CO2**
Q7	(a) Determine the operating point of the given amplifier as shown in Fig 3 under DC analysis? Evaluate the following performance parameters of the given CE amplifier below (b) Find *Zi* and *Zo*. (c) Calculate *Av* and *Ai*.  Fig 3	**10**	**C03**
Q8	(a)Analyze the Characteristics of Enhancement type and Depletion type MOSFET? (b)Draw the transfer and output characteristics of N- channel JFET and elaborate on the input impedance of the JFET? ***OR*** Compute the Gate capacitance C_G, gate to drain capacitance C_{GD}, gate to source capacitance for the Fig. 4. Consider the overlapping capacitances $C_{GSO} = C_{GDO} = 5$ fF/m^2 .What will be effects on these capacitances when horizontal dimension are scaled by 1/4 and vertical dimensions by 1/3.	**10**	**CO2**

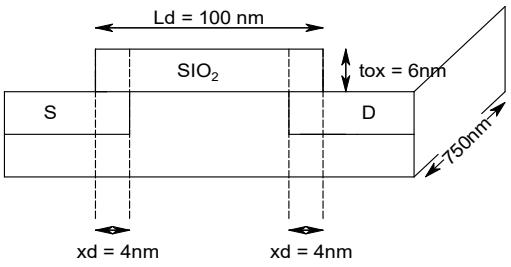
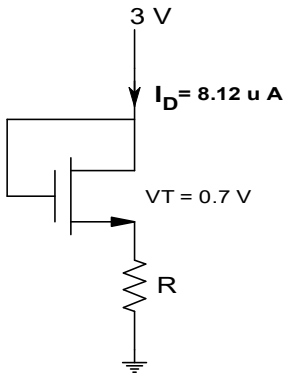
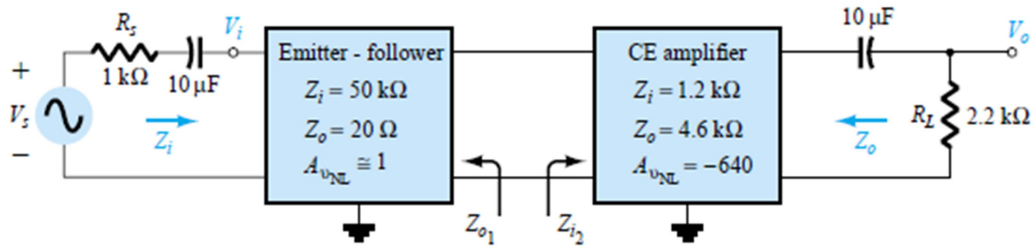
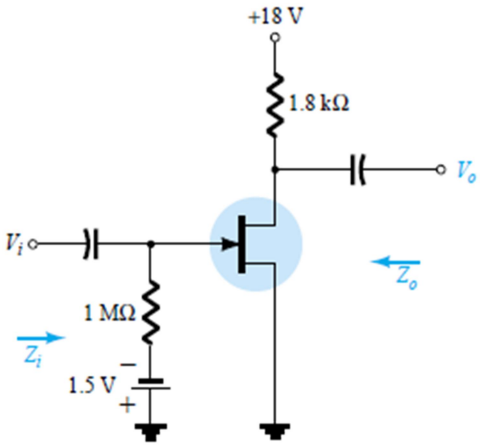
	 Fig. 4		
Q9	Determine the value of resistance R in the below circuit (Fig. 5) for the 180 nm technology where W/L = 4 and gate oxide capacitance formed by dielectric = 20 $\mu F/m^2$oxide thickness (electron mobility = 1200 cm^2/Vs)?  Fig. 5	**10**	**C03**
	SECTION-C (2x20=40 M)		
Q10	Consider the BJT amplifier shown below (Fig. 6) and determine the followings: (a) Calculate *Zi* and *Zo*. (b) Find Over all *Av* and *Ai*. (c) Calculate the output for V_i = 250m.Sin2π100t. (d) Draw the Gain Frquecny spectrum of the given amplifer. 	**20**	**CO4**

	Fig. 6		
Q11	The fixed-bias common source configuration having an operating point defined by VGS_Q = 2 V and ID_Q = 5.625 mA, with ID_{SS} = 10 mA and VGS_{OFF} = -8 V. The network configuration is shown in Fig. 7 with an applied input signal *Vi*. The value of *Yo* is provided as 50 µS. (a) Determine *gm*. (b) Find *rd*. (c) Determine *Zi*. (d) Calculate *Zo*. (e) Determine the voltage gain *Av*.  Fig. 7 **OR** (a) Explain why it is important to set the Q point at the middle of the DC load line. Draw the proper DC load line on output characteristics for common emitter configuration (b) Describe the thermal run away condition in BJTs and how it affects the operating point of an amplifier.	**20**	**CO3**