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UPES
End Semester Examination, December 2023

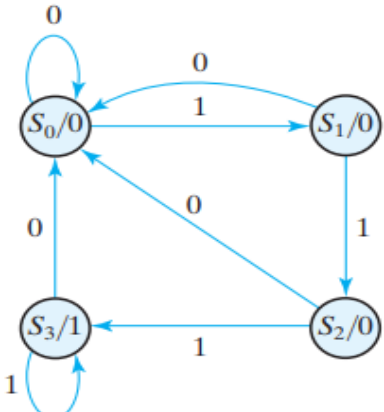
Program Name: Electronics & Communication Engineering/ Electronics & Computer Engineering Semester: III
Course Name: Digital System Design Time: 3 hrs
Course Code: ECEG-2037 Max. Marks: 100
Nos. of page(s): 2 Instructions: Assume any data in the design, if required.

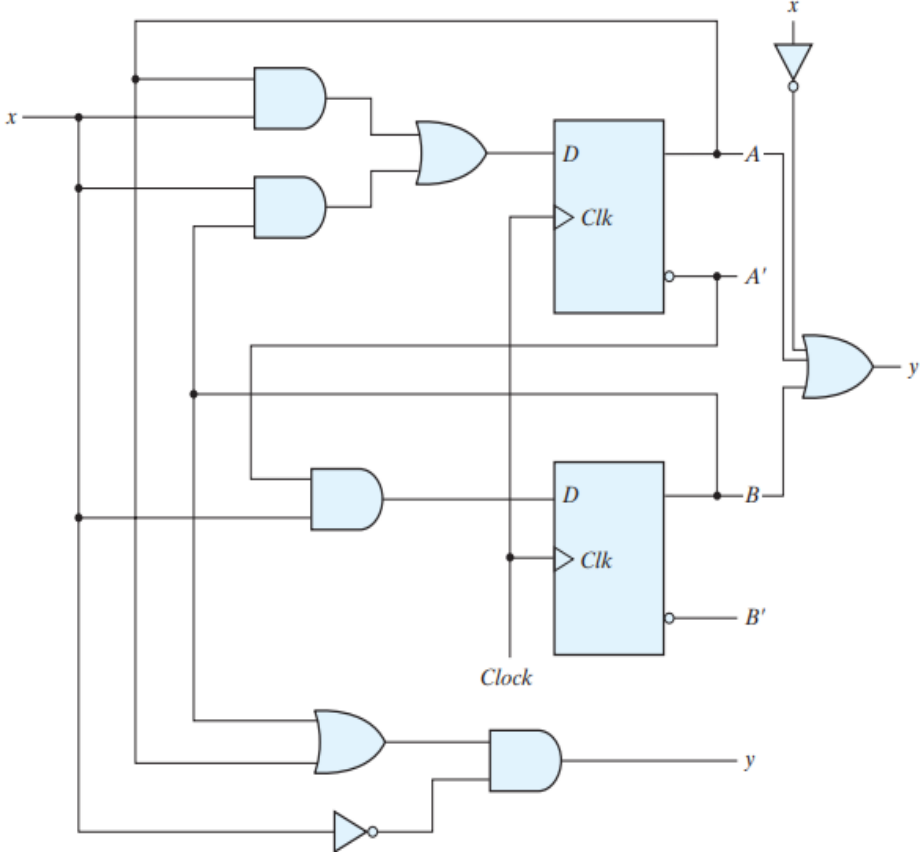
SECTION-A (5Q x 4M = 20 Marks)

S. No.	Question	Marks	CO
Q.1	Explain the followings with example for digital logic families. (a) Fan-in (b) Fan-out (c) Propagation delay (d) Noise Margin (e) Power dissipation	5	CO4
Q.2	Discuss the functionality of JK flip-flop with truth table, characteristics table, equation and support design using NAND and NOR logic.	5	CO3
Q.3	Explain the functionality and logic diagram of the (3 x 8) decoder.	5	CO2
Q.4	Solve the following function minterms using 5-variable K-MAP directly or the Tabulation method. $f(A, B, C, D, E) = \sum (m_0, m_2, m_5, m_7, m_8, m_{10}, m_{16}, m_{21}, m_{23}, m_{24}, m_{27}, m_{31})$	5	CO1

SECTION B (4Q x 10M = 40 Marks)

Q.5	Design a code converter that accepts 4-bit gray code as inputs and provides 4-bit binary output.	10	CO2
Q.7	Detail the ECL logic family for non-saturated logic with complete description of the logic circuit and operation. How is it applicable for wired logic, AND, and OR operation? <p style="text-align: center;">OR</p> Design a 4-bit multiplier with complete description of functionality, truth table, and logic diagram that accepts two inputs. Input $A = A_3A_2A_1A_0$ input $B = B_3B_2B_1B_0$	10	CO4
Q.8	What is the difference between Mealy and Moore FSM? The state diagram of a Moore FSM is shown. Design the FSM using D/JK flip-flop.	10	CO3



<p>Q.9</p>	<p>A sequential circuit is defined using the following logic diagram. Determine the following.</p> <p>(a) State transition equations (b) State Table (c) State diagram</p>  <p>The logic diagram shows two D flip-flops. The top flip-flop has its D input connected to $x \cdot (x \oplus A)$ and its clock input to $x \oplus A$. Its outputs are A and A'. The bottom flip-flop has its D input connected to $x \cdot A$ and its clock input to $x \oplus A$. Its outputs are B and B'. There are two outputs labeled y. The first y is $A \oplus B$. The second y is $x \oplus (A \cdot B)$.</p>	<p>10</p>	<p>CO3</p>
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SECTION-C (2Q x 20M = 40 Marks)

Attempt any two of the following

<p>Q.10</p>	<p>Convert/implement the following.</p> <p>(a) JK flip-flop to D Flip-Flop (b) D- Flip-Flop to T-flip-flop (c) Full adder using the decoder (d) Multiplexer (16x1) using (4x1) multiplexer</p>	<p>20</p>	<p>CO2</p>
<p>Q.11</p>	<p>(a) Compare the functionality of PAL, PLA, and PROM technology for PLDs. Implement the full subtractor function using PAL, PLA, and PROM.</p> <p>(b) Design BCD Adder using 4-bit binary adder and detail the complete behavior with equation and truth table</p>	<p>10+10</p>	<p>CO1</p>
<p>Q.12</p>	<p>(a) Design a mod-12 synchronous counter using JK Flip-Flop.</p> <p>(b) What are the different operations of the shift register? Detail the operation of the 4-bit shift register, logic diagram with timing diagram for any one operation.</p>	<p>15+5</p>	<p>CO3</p>