Name: **Enrolment No:**	

UPES

End Semester Examination, May 2024

Programme Name : B. Tech (Electronics and Computer) Semester : II
Course Name : Analog Electronics-I Time: 03 hrs
Course Code : ECEG1011 Max. Marks: 100
Nos. of page(s) : 3

Instructions: In Section B and C, one internal choice is provided for each.

SECTION A

Answer all questions.

S. No.		Marks	CO
Q 1	State the True/False (i) Bypass capacitors in an amplifier determine the high-frequency response. (ii) An octave corresponds to a doubling of the frequency. (iii) The drain current in a CS amplifier can be calculated using a Shockley equation. (iv) Base bias is less stable than voltage-divider bias.	**4**	**CO1**
Q 2	(i) In an FET, the trans-conductance g_m is proportional to (a) I_{DS} (b) I_{DS}^2 (c) $\sqrt{I_{DS}}$ (d) $\frac{1}{I_{DS}}$ (ii) A certain common-source amplifier has a voltage gain of 10. If the source bypass capacitor is removed, (a) the voltage gain will increase (b) the transconductance will increase (c) the voltage gain will decrease (d) the Q-point will shift. (iii) If the voltage gain doubles, the decibel voltage gain increased by (a) A factor of 2 (b) 3 dB (c) 6dB (d) 10 dB (iv) A Darlington transistor has (a) A very low input impedance (b) Three transistors (c) A very high current gain (d) One V_{BE} drop	**4**	**CO1**
Q 3	Describe the advantages and disadvantages of FET in comparison to BJT.	**4**	**CO1**
Q 4	A four identical amplifier has a lower 3 dB frequency for an individual stage of f_L = 40Hz. What is the value of f_L^* for this full amplifier.	**4**	**CO4**
Q 5	It desired to have a high gain amplifier with high input impedance and low output impedance. If a cascade of four stages is used, what configurations should be used for each stage?	**4**	**CO4**
	SECTION B		
Q 6	Show that the transconductance, g_m of a JFET is related to the drain current I_{DS} by $g_m = \frac{2}{\lvert V_p \rvert}\sqrt{I_{DSS} I_D}$ If V_P = - 4V and I_{DSS} = 4 mA, plot g_m versus I_D.	**10**	**CO3**
Q 7	Sketch the small-signal low frequency r_e model of a common emitter BJT configuration. Determine Z_i, Z_o, and A_v for the given configuration.	**10**	**CO3**
Q 8	Draw the Darlington pair circuit. Explain why the input impedance is higher than that of a single stage emitter follower. **OR**	**10**	**CO4**

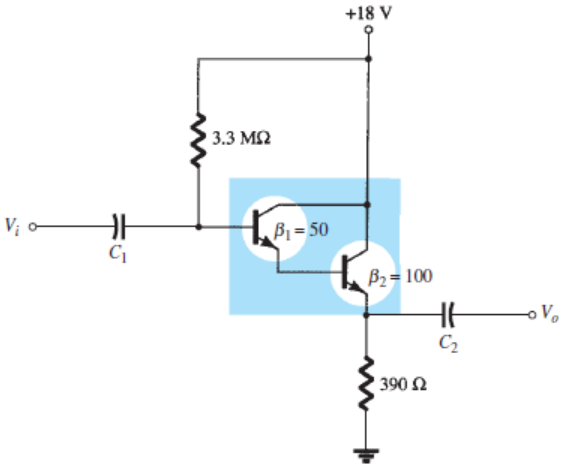
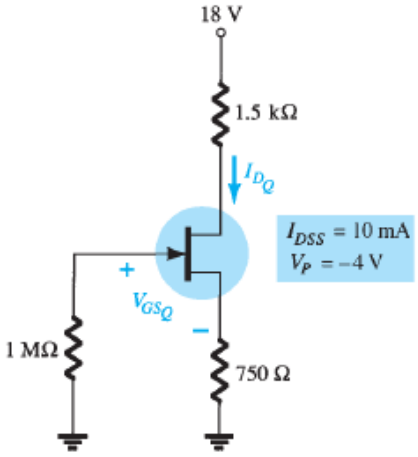
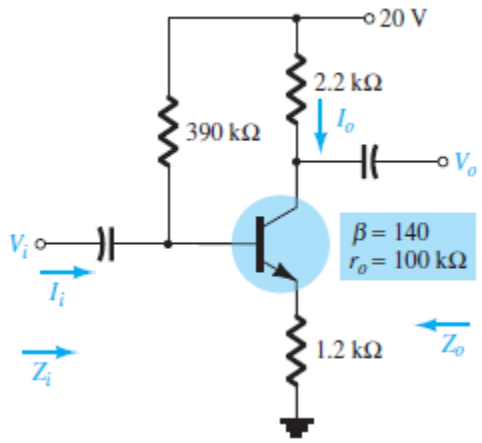
	Calculate the dc bias voltages and currents for the Darlington configuration of Fig.1  **Fig.1**		
Q 9	Sketch the transfer and drain characteristics of an n-channel JFET with I_{DSS} = 9 mA and V_P = -6 V for a range of V_{GS} = -V_P to V_{GS} = 0 V.	**10**	**CO2**
	SECTION C		
Q 10	(i) Explain the construction of n-channel JFET. (ii) Differentiate between (a) n-channel and p-channel MOSFET. (b) Depletion type and enhancement type MOSFET. (iii) For the network of Fig.2, determine: (a) V_{GSQ} and I_{DQ}. (b) V_{DS}, V_D, V_G, and V_S.  **Fig.2**	**5+5+10**	**CO1** **CO2**
Q 11	For the network of Fig.3 (a) Determine r_e. (b) Find Z_i and Z_o. (c) Calculate A_v. (d) Repeat parts (b) and (c) with r_o = 20 kΩ	**4x5=20**	**CO3**

Fig.3



OR

The self-bias configuration of Fig.4 has an operating point defined by V_{GSQ} = -2.6 V and I_{DQ} = 2.6 mA, with I_{DSS} = 8 mA and V_P = -6 V. The value of g_{os} is given as 20 mS.

(a) Determine g_m.
(b) Find r_d.
(c) Find Z_i.
(d) Calculate Z_o with and without the effects of r_d. Compare the results.
(e) Calculate A_v with and without the effects of r_d. Compare the results.

5X4=20

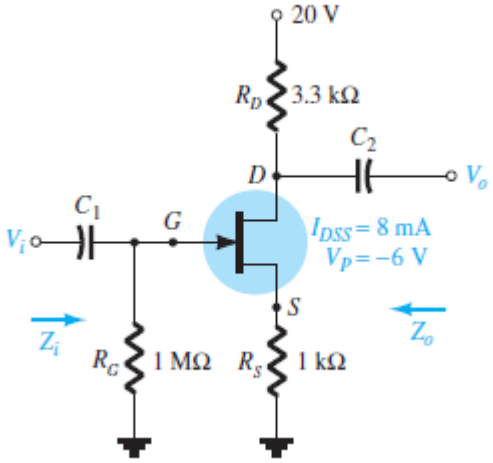


Fig.4