Name: **Enrolment No:**	

UPES

End Semester Examination, May 2024

Course: Computer Organization and Architecture **Semester: II**

Program: B.TECH CSE **Time : 03 hrs.**

Course Code: CSEG 1032 **Max. Marks: 100**

Instructions: Draw DIAGRAMS with pencil

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Represent $(105.625)_{10}$ in (a) IEEE single precision format (or) (b) IEEE double precision format	**4**	**CO1**
Q 2	Explain the following in brief: (i) ReRAM (ii) Phase Change Memory	**4**	**CO3**
Q 3	Define principle of locality in computer architecture? What are its main aspects?	**4**	**CO4**
Q 4	Differentiate between Shared and Isolated I/O.	**4**	**CO3**
Q 5	What is a vector processor and an array processor? Explain briefly with suitable examples.	**4**	**CO5**

SECTION B
(4Qx10M= 40 Marks)

Q 6	Discuss the various addressing modes used in computer instruction sets. Explain how each addressing mode operates and provide examples of instructions utilizing different addressing modes.	**10**	**CO2**
Q 7	Outline the stages of the instruction cycle in a CPU, detailing each stage's purpose and operation. Provide examples of typical interrupts and their impact on the execution flow of a program.	**10**	**CO2**
Q 8	With DMA module diagram explain the working of direct memory access method for data transfer to and from the peripherals.	**10**	**CO4**
Q 9	Explain Associative memory with the help of a suitable block diagram. Give a suitable example explaining how the argument data is searched within the associative memory.	**10**	**CO3**

	Consider a direct mapped cache of size 16KB with block size 256 Bytes. The size of main memory is 128KB. Find (i) Number of bits in Tag (ii) Tag directory size OR Based on memory, how many types are multiprocessors divided into? Explain each type with block diagrams.		
SECTION-C (2Qx20M=40 Marks)			
Q 10	(a) A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. What are the number of bits for the TAG field? (b) Define Flynn's taxonomy of computer architecture? Explain in detail the various architecture based on Flynn's classification.	**10+10**	**CO3**
Q 11	(a) We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions? Assume zero delay in the register. (b) With neat architectural diagrams highlight the major differences, pros and cons between hardwired control unit and programmed control unit? OR (c) Explain how the address of the next microinstruction is selected with the help of a flowchart. (d) A memory system consists of cache and main memory. If it takes 1 cycle to complete a cache hit and 100 cycle to complete a cache miss. What is the average memory access time if the hit rate in the cache is 97%.	**10+10**	**CO5**