Name: **Enrolment No:**	

UPES

End Semester Examination, December 2024

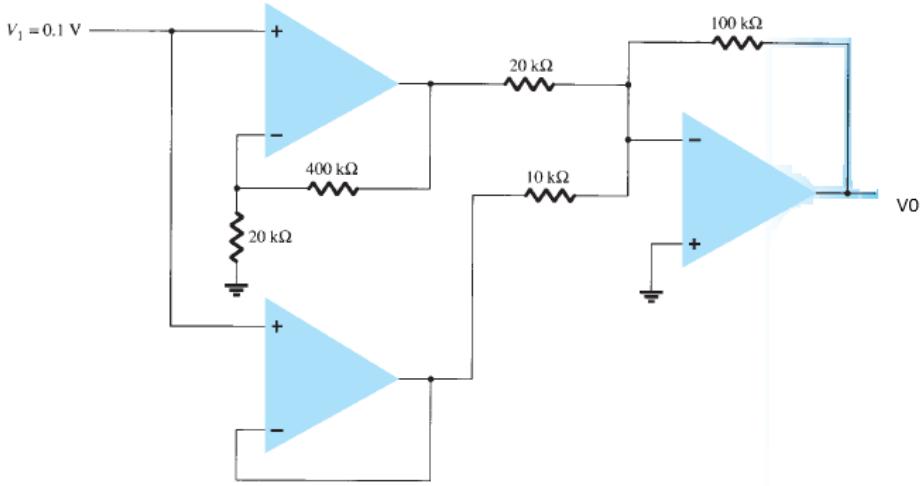
Programme Name: B.Tech. (Electronics and Computer Engineering). Semester : III
Course Name : Analog Electronics-II Time: 03 hrs
Course Code : ECEG 2065 Max. Marks: 100
Nos. of page(s) : 2

Instructions: In Section B and C, one internal choice is provided in Q.9 and Q.11, respectively.

SECTION A

Answer all questions.

S. No.		Marks	CO
Q 1	Multiple choice question (a) A summing amplifier can have (i) only one input (ii) only two inputs (iii) any number of inputs (iv) none of these (b) In a zero-level detector, the output changes state when the input (i) is positive (ii) is negative (iii) crosses zero (iv) has a zero rate of change. (c) The bandwidth of an ac amplifier having a lower critical frequency of 1 kHz and an upper critical frequency of 10 kHz is (i) 1 kHz (ii) 9 kHz (iii) 10 kHz (iv) 11 kHz . (d) Common-mode gain of a practical operational amplifier is (i) very high (ii) very low (iii) always unity (iv) unpredictable	4	CO1
Q 2	State True/False (a) The gain-bandwidth product of an Op-Amp remains constant regardless of the frequency. (b) A Schmitt Trigger is used to eliminate noise from input signals by providing hysteresis. (c) A low-pass filter using an Op-Amp allows high-frequency signals to pass while attenuating low-frequency signals. (d) The common-mode rejection ratio (CMRR) of an ideal Op-Amp is zero.	4	CO1
Q 3	An Op-Amp has a slew rate of 0.5 V/μs. If the input signal changes by 2V, calculate the minimum time required for the output to follow the input change. Show all steps of calculation.	4	CO1
Q 4	An operational amplifier has a differential gain (A_d) of 2500 and a common-mode gain (A_{cm}) of 0.50. Calculate the CMRR in both ratio form and in decibels (dB). Show all steps of the calculation.	4	CO1
Q 5	An A/D converter has a resolution of 8 bits and an input voltage range of 0 V to 5V. Calculate the smallest voltage change that can be represented by this converter. Show all steps of the calculation.	4	CO3
	SECTION B		
Q 6	(a) Explain the working principle of a phase shift oscillator using an operational amplifier. Draw its circuit diagram and describe how the required phase shift is achieved. (b) Design a phase shift oscillator to generate a frequency of 500 Hz. If the resistors are all equal (R) and the capacitors are identical (C), calculate the values of R and C. Show all steps of the calculation.	**5** **5**	CO2 CO4

Q 7	Determine the output voltage V_0 for the given circuit. Provide all intermediate steps involved in the calculations.  	10	CO2
Q 8	Draw a neat, labeled circuit diagram of a voltage series feedback amplifier. Derive expressions for the amplifier's closed-loop gain, input impedance, and output impedance, showing how they are affected by the feedback.	10	CO2
Q 9	(a)Explain the working of a Schmitt Trigger circuit using an Op-Amp. Draw the circuit diagram and describe its significance in noise reduction. (b) A Schmitt Trigger has a supply voltage V_{CC}=10V, with resistors R_1= 10kΩ and R_2= 90kΩ. Calculate the upper and lower threshold voltages. **OR** Draw the circuit diagram of a voltage-to-current converter with ground load. Show that the load current depends on the input voltage v_{in} and input register R.	10 10	CO2
	SECTION C		
Q 10	(a) Explain the operation of a 555 timer in monostable mode. Draw the circuit diagram and describe one practical application. (b) A 555 timer is used in monostable mode with a resistor $R = 5\ k\Omega$ and a capacitor C=10 μF. Calculate the pulse width of the output signal.	10	CO3
Q 11	(a) Draw a clear, labeled circuit diagram of a wide band-reject filter. Additionally, illustrate its frequency response, highlighting the lower and upper cutoff frequencies. (b) Design a wide band-reject filter with $f_H = 200\ Hz$, $f_L = 1000\ Hz$, and pass-band gain of 2. Also draw an approximate frequency response plot for the filter. **OR** (a) Draw a labeled circuit diagram of a sample and hold circuit. Additionally, illustrate its input and output waveforms, explaining how the circuit functions during the sampling and holding phases. (b) Draw a labeled circuit diagram of a 4-bit D/A converter using a binary-weighted resistor network. Create a table showing the output voltage corresponding to each 4-bit binary input.	10 10 10 10	CO3 CO4 CO3 CO3